CONTROL DATA

60000132

Virtual State
Hardware Reference
Volume 1

REFERENCE Guide

/ CYBER 960/962
Computer System

CYBER 960/962 Computer Systems
Virtual State Volume 1

Hardware Reference

This product is intended for use only as described in this document. Control Data cannot be responsible for the proper functioning of undescribed features and parameters.

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About This Manual

This manual contains hardware reference information for the CDC® CYBER® 960 and 962 Computer Systems in their Virtual State of operation.

The manual provides model-dependent information regarding the system description and functional descriptions of the computer system's hardware.

Audience

This manual is for use by customer, marketing, and training personnel who want a general yet technical description of the computer system.

Organization

Chapter 1 introduces the CYBER 960 and 962 computer systems, identifies their physical and functional characteristics, and provides descriptions of their major system components.

Chapter 2 introduces the central processing unit (CPU) operating states and modes of operation, and discusses dual-CP operation. It provides functional descriptions of the central processor (CP), central memory (CM), and central memory control (CMC), which are contained in the CPU, as well as the power unit and input/output unit (IOU).

Conventions

New features, as well as technical changes, deletions, and additions to this manual, are indicated by vertical bars in the margins.

FCC Compliance

This equipment generates, uses and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device (insert peripheral computing device if appropriate) pursuant to Subpart J of Part 15 of the FCC Rules which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

Related Manuals

Additional hardware reference information regarding operation of the computer systems in both their CYBER 170 State and Virtual State environments is available in manuals shown in the hardware manuals figure on the following page.

CYBER 960/962 HARDWARE MANUALS

SYSTEM MANUALS

Site Preparation

- General Information Site Preparation — 60275100
- Mainframe Complex Data Site Preparation — 60000119
- Peripheral Equipment Data Site Preparation — 60275300

Installation

- Mainframe Installation and Checkout — 60000120

Operation

- Virtual State Reference Volume 1 — 60000132
- Virtual State Reference Volume 2 — 60000133
- CYBER 170 State Reference — 60000127
- 19003 System Console Operations/ Maintenance — 60463610

Troubleshooting

- System Troubleshooting — 60000122

Codes

- System Codes Booklet — 60458100

EQUIPMENT MANUALS

Central Processing Unit (CPU)

- CPU Maintenance — 60000123
- CPU Theory and Diagrams — 60000118

Mainframe Power and Environmental

- Mainframe Power and Environmental Subsystem Maintenance — 60000125
- Mainframe Power and Environmental Subsystem Theory and Diagrams — 60000121

Input/Output Unit (IOU)

- IOU Maintenance — 60000130

CYBER 960 IOU Manuals

- IOU Theory and Diagrams Levels 0-3 — 60463540
- IOU Diagrams Level 4 — 60462210
- Wire Lists Microfiche — 60000134

CYBER 962 IOU Manuals

- IOU Theory and Diagrams Levels 0-3 — 60000235
- IOU Diagrams Level 4 — 60000236
- Wire Lists Microfiche — 60000135

Motor Generator (MG) Equipment

- 25-kVA Frequency Converter Hardware Maintenance — 60456520
- 40-kVA Control Cabinet and Motor Generator Hardware Maintenance — 60454720
- MG Interface Unit Installation and Maintenance — 60000124

M02240

Additional Related Manuals

Other manuals applicable to the CYBER 960 Series of computer systems are:

Title	Publication Number
NOS Version 2 Operator/Analyst Handbook	60459310
NOS Version 2 Systems Programmer's Instant	60459370
NOS Version 1 Operator's Guide	60457700
NOS Version 1 Systems Programmer's Instant	60457790
NOS/VE Analysis Usage	60463915
NOS/VE Operations Usage	60463914
CYBER Initialization Package (CIP) Reference Manual	60457180
CYBER 15x Offline MSL Reference Manual	60456530

Publication ordering information and latest revision levels are available from the Literature Distribution and Services catalog, publication number 90310500.

Ordering Manuals

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System Description 1

This chapter:

- Introduces the CYBER 960 and 962 computer systems
- Identifies the physical characteristics of the system
- Provides an overview of the CYBER 960 and 962 products
- Identifies the functional characteristics of the system
- Provides descriptions of the major system components

Introduction

CYBER 960 and 962 are large-scale, high-speed computer systems for both business and scientific applications. Figure 1-1 shows the basic CYBER 960/962 configuration. Both systems include the following components.

- Power unit
- Central processing unit (CPU)
- Input/output unit (IOU)
- System console (purchased as separate product)

The CYBER 960 system contains 20 nonconcurrent input/output (NIO) peripheral processors (PPs) and 24 CYBER 170 channels, and is capable of dual-state operation, that is, may execute in either a Virtual State environment or a CYBER 170 State environment. (Refer to Functional Characteristics later in this chapter.)

The CYBER 962 contains only concurrent input/output (CIO) PPs with direct-memory-access (DMA) channels, and operates in Virtual State only.

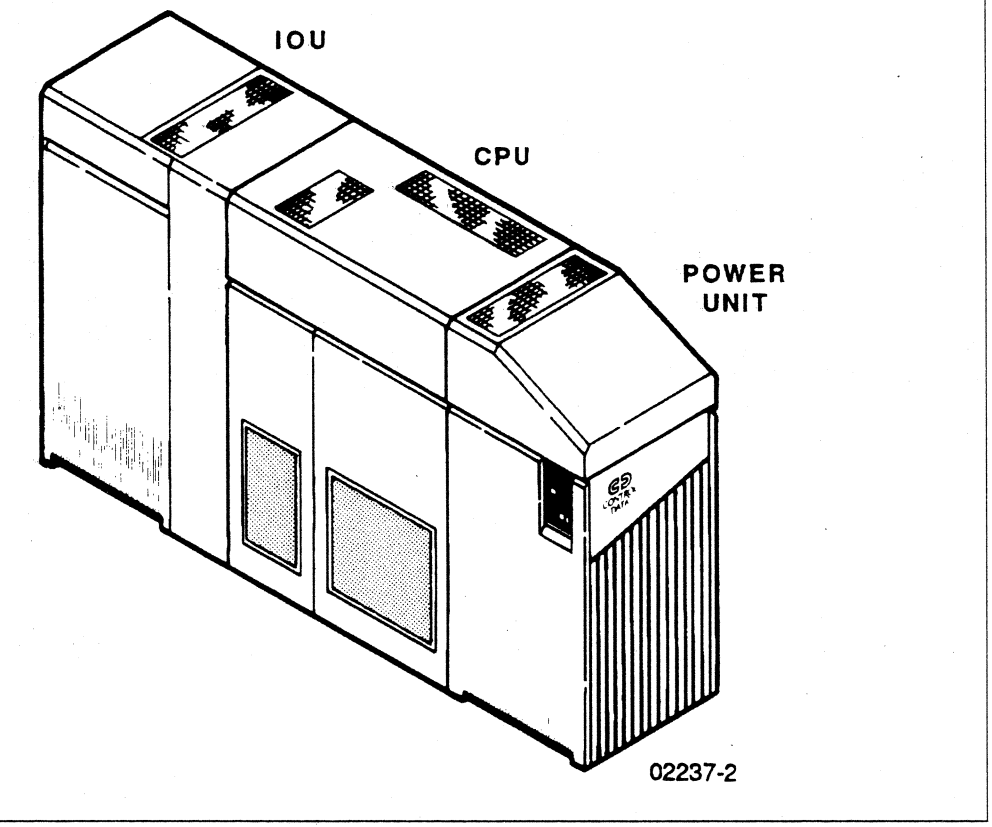

Figure 1-1. CYBER 960/962 Configuration

Physical Characteristics

The mainframe configuration for CYBER 960 and 962 computer systems include:

- Power unit
- CPU, which contains the central processor (CP), central memory (CM), and central memory control (CMC)
- One or more IOUs
- System console

Three configurations of CPs are available for either the CYBER 960 or 962 system. The processing speed of the basic CP can be enhanced with a high performance option, and a second CP option, adding an independently-operating CP, is available. These are indicated by the model number of the product.

- CYBER 960-11 or CYBER 962-11 - base performance, single CP
- CYBER 960-31 or CYBER 962-31 - enhanced performance, single CP
- CYBER 960-32 or CYBER 962-32 - enhanced performance, dual CP

In addition to the CP configurations, several IOU options are available to enhance I/O processing. The additional IOUs are the same for both the CYBER 960 and 962 system. The base CYBER 960 IOU contains 20 NIO PPs and 24 CYBER 170 channels. The base CYBER 962 IOU contains 10 CIO PPs and 8 DMA channels. Each DMA channel can operate in intelligent standard interface (ISI), intelligent peripheral interface (IPI), or CYBER 170 protocol.

As an extension of the system cabinet, one or two additions of five CIO PPs and five DMA channels are available. A separate standalone IOU cabinet can contain 10, 15, or 20 CIO PPs with 10, 15, or 20 DMA channels. All PPs interface to the same CM as the CP(s).

The base CM contains 32M bytes of RAM (64M bytes for CYBER 960). CM upgrades allow the following memory sizes.

- 64M bytes
- 128M bytes
- 192M bytes
- 256M bytes

Figure 1-1 shows the basic system configuration. Figure 1-2 shows the expanded system with the maximum IOU configuration.

All CYBER 960 and 962 equipment is cooled by forced air.

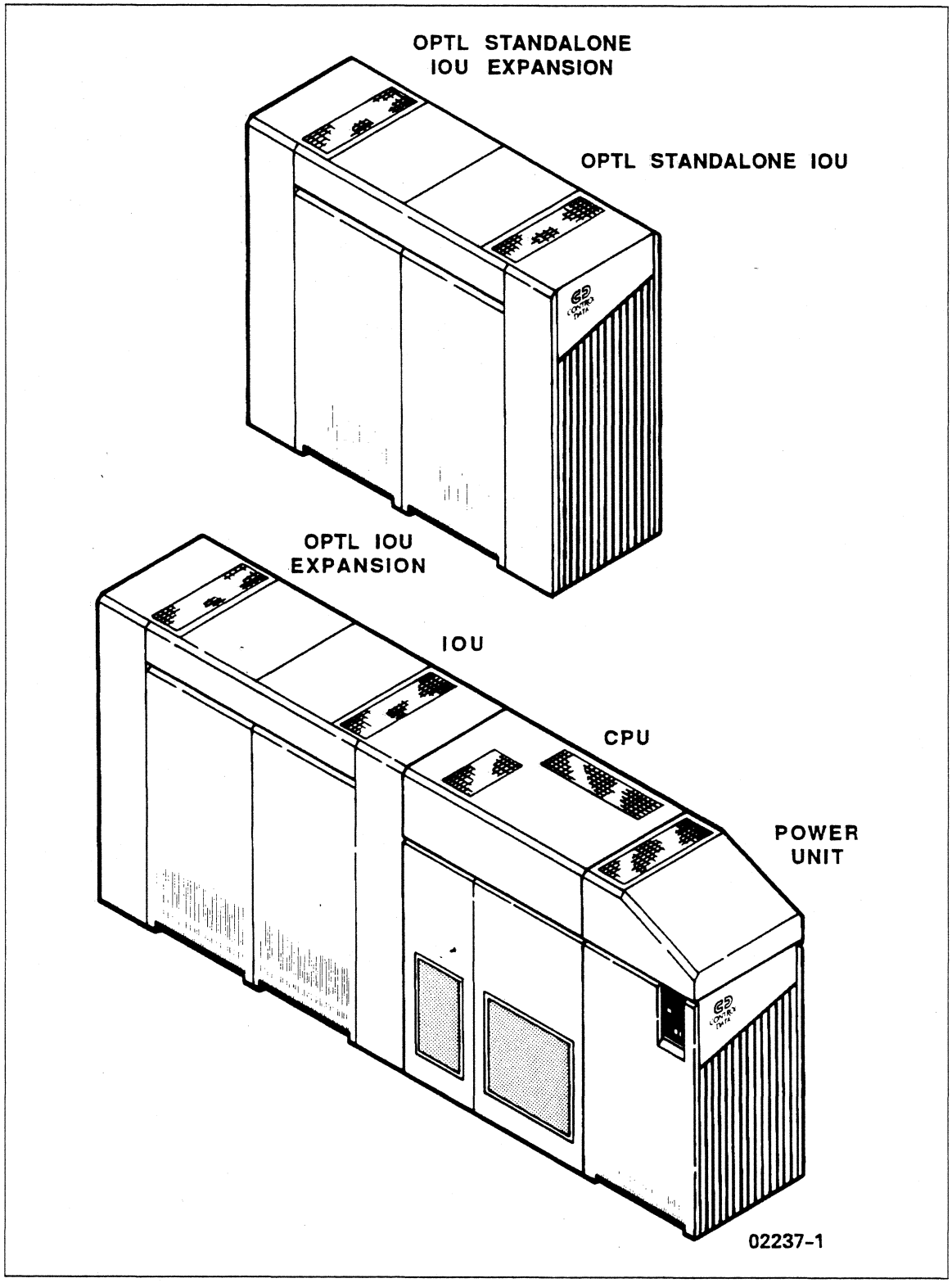

Figure 1-2. CYBER 960/962 with Maximum IOU Configuration

Product Overview

The CYBER 960 Series of computer systems is offered with a broad range of product options designed to meet the unique performance needs of Control Data's diverse customer base. Products offered with the CYBER 960 Series are classified either as required options or upgrade options.

Required Options

Required options are products needed to support the basic functioning of the CYBER 960 or 962 mainframe. Included in this category are the system console, the motor-generator (MG) set, and the MG interface unit. Table 1-1 provides the product numbers and descriptions of the required options.

Table 1-1. Required Product Options

Product Number	Description
System Console	
• 19003-1 or	Attaches to the CYBER 960 IOU and is used to initialize the system, initiate system operations, and run diagnostic programs for maintenance purposes.
• 19003-2	Attaches to the CYBER 962 IOU (or to the optional standalone IOU in a CYBER 960 system) and is used to initialize the system, initiate system operations, and run diagnostic programs for maintenance purposes.
MG Interface Unit	
• 19405-1	Provides status and control link between the MG set (or frequency converter) and the CYBER 960/962 power unit; also allows for remote adjustment of MG power phases from the computer room.
Frequency Converter or MG Set	
• 10513-725 or	25-kVA frequency converter, converts 60-Hz power to 400 Hz.
• 10513-740 or	40-kVA MG set, converts 60-Hz power to 400 Hz.
• 10514-725 or	25-kVA frequency converter, converts 50-Hz power to 400 Hz.
• 10514-740	40-kVA MG set, converts 50-Hz power to 400 Hz.

Upgrade Options

Upgrade options are products that can be added to a CYBER 960/962 system to improve its input/output capacity, increase its memory, and enhance its processing performance capability. Figure 1-3 shows CYBER 960 Models 11, 31, and 32 configurations and the available upgrade options. Figure 1-4 shows CYBER 962 Models 11, 31, and 32 configurations and the available upgrade options.

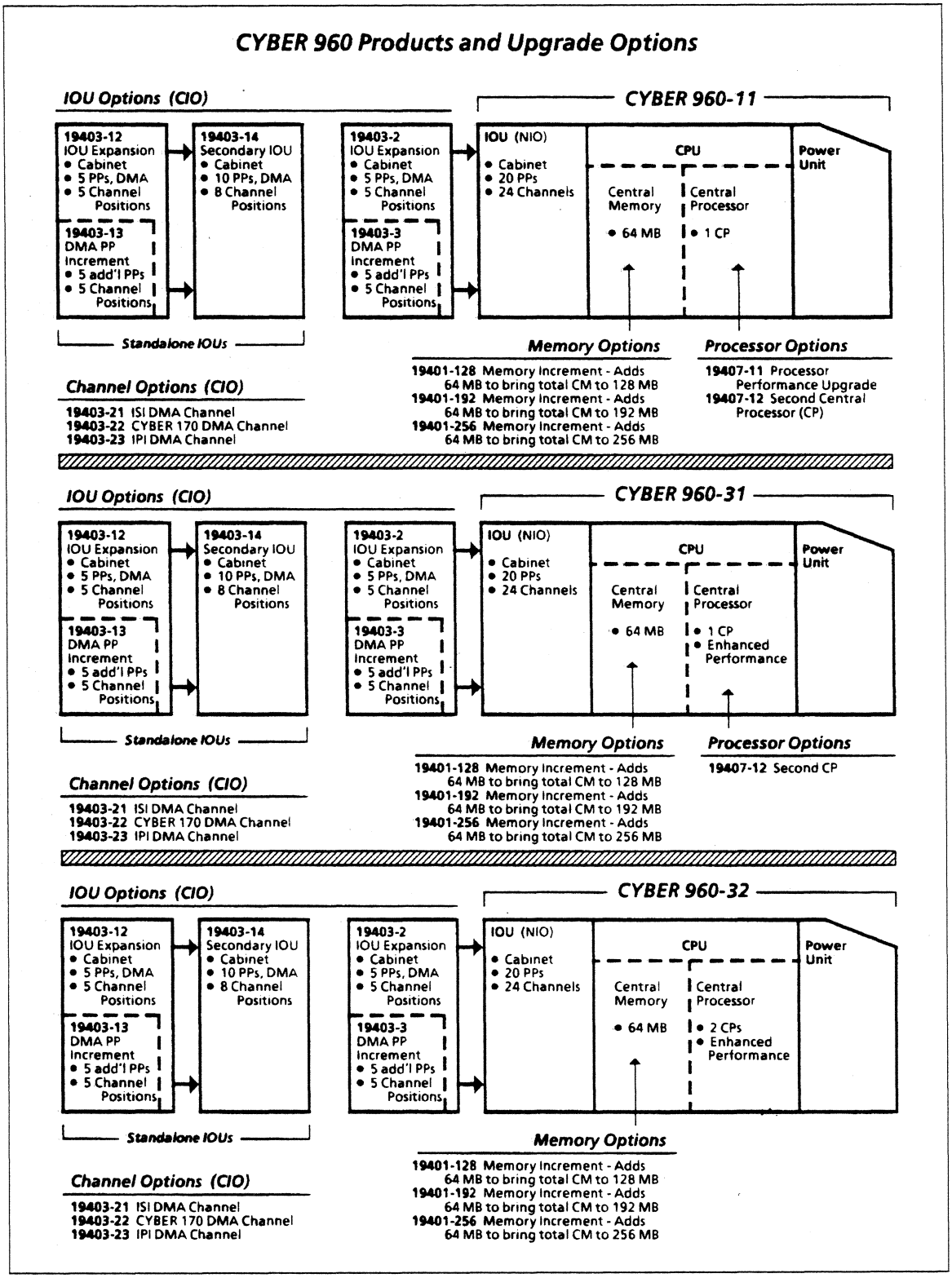

Figure 1-3. CYBER 960 Products and Upgrade Options

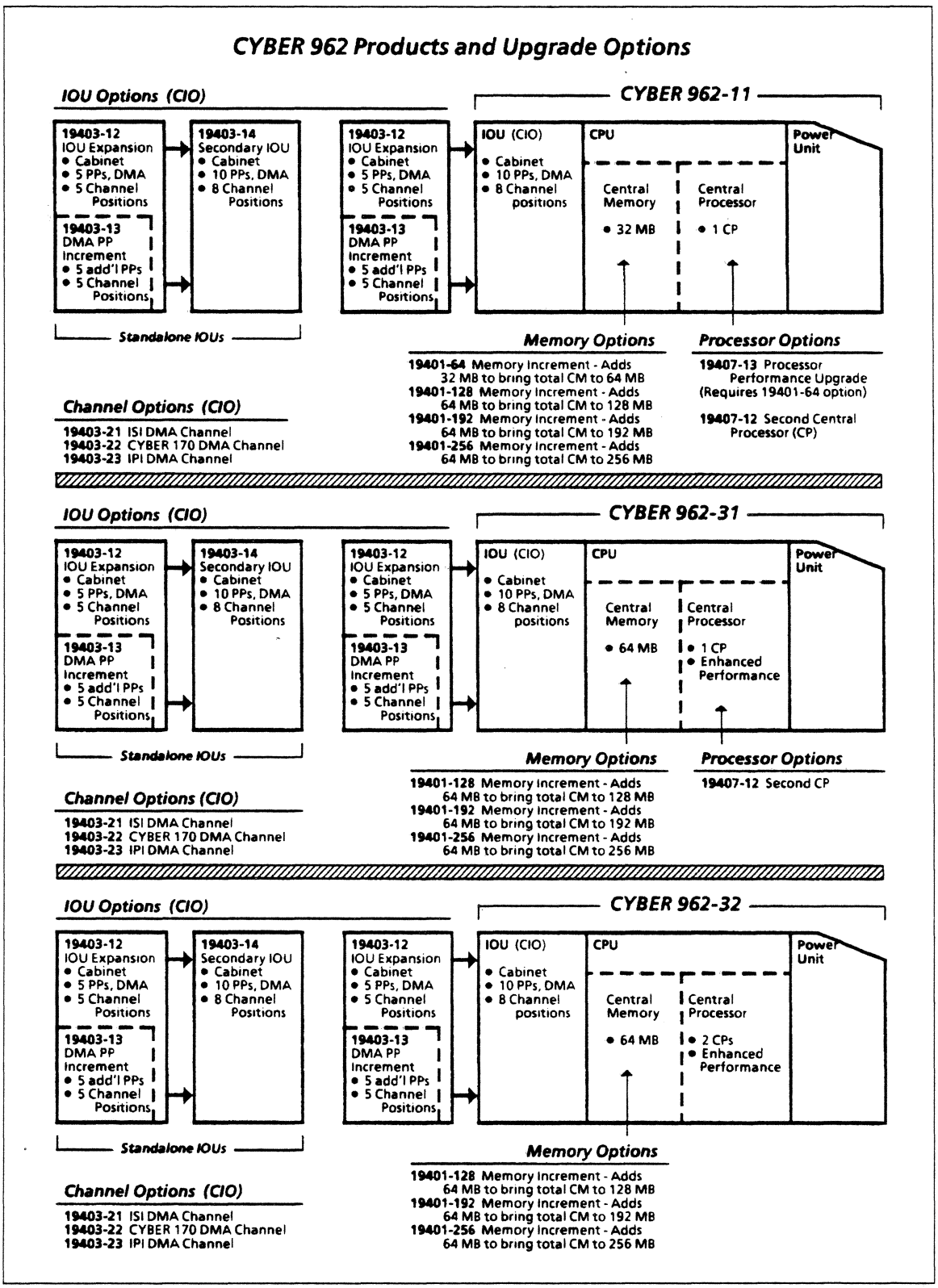

Figure 1-4. CYBER 962 Products and Upgrade Options

Functional Characteristics

To achieve high computation speeds, the CYBER 960 and 962 computer systems use emitter-coupled logic (ECL) and large-scale integration (LSI) logic.

The semiconductor memory is divided into eight independent banks to minimize conflicts among CM requests. All eight banks may be simultaneously completing read and write requests.

High speed is also the objective of the CP design. The CP design is based on the assumption that instructions and data are both accessed, in most cases, accessed from successive memory locations. Accordingly, the CP prefetches both instructions and data expected to be used next while the current instruction is being processed.

System I/O speeds are determined by the capabilities of existing external devices.

The CYBER 960 CP supports two states of operation. The CYBER 962 CP supports only Virtual State operation.

Virtual State	Operation as a computer with virtual-memory byte addressing, using the Virtual State instruction set and data formats. Virtual State is the native operating state of the CP.
CYBER 170 State	Operation as a computer with real-memory word addressing, using CYBER 170 State CP instruction set and data formats.

The Virtual State and CYBER 170 State environments may be present in the CYBER 960 at the same time with the CP executing in either environment. Network Operating System/Virtual Environment (NOS/VE) is the operating system of Virtual State; the Network Operating System (NOS) is the operating system of CYBER 170 State.

Refer to the CYBER 170 State Hardware Reference Manual listed in the hardware manual set figure under Related Manuals for more information about 170 State operation.

CP General Functional Characteristics

The following CP characteristics are common to both Virtual State and CYBER 170 State.

- 32K-bytes cache buffer memory, with data lookahead
- 44.8-ns cache access time
- Instruction lookahead and branch instruction prediction to maintain a continuous stream of instructions for execution
- Separate arithmetic units for fixed-point and floating-point (FP) binary and decimal data processing
- Hardware data format checking, conversion, and editing
- CMC to control data flow between CM and system components
- Extensive parity checking on data and address paths
- 11.2-ns clock period

CP Virtual State Functional Characteristics

The following CP characteristics are exclusive to Virtual State.

Main Registers

The following CP registers hold most of the operands and addresses used for computational purposes.

- Sixteen 48-bit address (A) registers
- One 64-bit program address (P) register
- Sixteen 64-bit operand (X) registers

Processing Capabilities

CP processing presents the following features.

- 64-bit internal word (8 bytes)
- Packed instructions (16/32-bit instructions in 64-bit words)
- Integer arithmetic (32/64-bit operands)
- FP arithmetic (12-bit exponent plus sign bit, 48/96-bit coefficient plus sign bit)
- Business data processing (BDP) (11 decimal data types and an alphanumeric data type supported by move/compare/edit instructions)
- Call and return mechanism

The other processing capabilities are:

- Load and store fields of 1 to 8 bytes
- Extract and insert strings of 1 to 64 bits
- Load and store multiple A and X registers
- Process immediate data from instruction word

Modes of Operation and Interrupts

The CP modes of operation and CP interrupt structure have the following characteristics.

- Monitor and job modes of operation
- Exchange instructions causing exchange of operating mode and executing process
- Trap interrupts on monitor mode conditions, with trap handled within present operating mode
- Trap interrupts on job mode conditions, with trap handled within present operating mode
- Exchange interrupts on job mode conditions, with an exchange to monitor mode for interrupt processing

Program Monitoring

CP program monitoring has five maskable classes of debug interrupts on up to 32 process virtual address (PVA) ranges.

Access Protection

The CP security features include the following characteristics.

- Controlled access to segments
- Fifteen rings of protection
- Segment locks and keys
- Eight types of segment access (read/write/execute with subdivisions)
- Controlled and protected entry points into shared code

CP CYBER 170 State Functional Characteristics

The CP has the following characteristics.

- 60-bit internal word
- Eight 60-bit operand (X) registers
- Eight 18-bit address (A) registers
- Eight 18-bit index (B) registers
- Two registers that isolate each user's CM space (RAC, FLC)
- Two registers that isolate each user's extended memory space (RAE, FLE)
- Register exchange instructions (exchange jumps) for interrupting programs
- FP arithmetic (10-bit exponent plus sign bit, 48-bit coefficient plus sign bit); some FP instructions use 96-bit (double-precision) coefficients.
- Integer arithmetic (60/18-bit operands)
- Character string compare/move facilities (6-bit characters)
- Packed instructions (15/30/60-bit instructions in 60-bit words)
- Synchronous internal logic
- Instruction and branch instruction lookahead
- Microcode control
- Parity checking of all major data and address paths
- Maintenance channel to IOU

Dual-CP System

Model 32 of the CYBER 960 and 962 systems supports a second CP. The dual-CP configuration has the following characteristics.

- On the CYBER 960-32, CP-0 supports both Virtual State and CYBER 170 State operation.
- On the CYBER 962-32, CP-0 and CP-1 support Virtual State operation only.
- Both CPs access a common queue of processes awaiting execution.
- Both CPs share Virtual State monitor mode and its interrupt handling routines.

CM Functional Characteristics

The CM has the following functional characteristics.

- 72-bit data word (64 data bits and 8 single-error correction/double-error detection [SECDED] bits)
- 4194K words (32M bytes) of metal-oxide semiconductor (MOS) dynamic random access memory (DRAM), with options available to 33 554K words (256M bytes)
- Organization of eight independent banks
- Directly addressable PVA space of up to 4096 segments, with up to 2 billion bytes per segment
- System virtual address (SVA) space of up to 65K segments
- Real-memory page size ranging from 2K to 64K bytes
- Bounds register to limit write access
- Read/write cycle time of 358.4 ns
- Partial write cycle time of 716.8 ns
- Maximum transfer rate of 1 word every 22.4 ns
- SECDED CM data verification
- Parity checking on all major data, address, and control paths
- Interleaved addressing
- Read and write data queuing

IOU Functional Characteristics

The CYBER 960 basic IOU is nonconcurrent, while the CYBER 962 basic IOU is concurrent. Both the basic IOUs have the following options available.

- IOU expansion
- Standalone IOU
- Standalone IOU expansion

These three IOUs are all functionally identical and are a subset of the standard concurrent IOU used with the CYBER 962. They are distinguished only by their physical orientation to the CPU. Figure 1-5 shows the various IOU configurations.

Standalone IOU Options

The optional standalone IOU configuration has the following characteristics.

- Expands the number of available CIO subsystem I/O channels
- Requires a system console
- Supports only Virtual State operation
- Accesses only IOU registers, using the maintenance channel
- Connects to CMC auxilary port

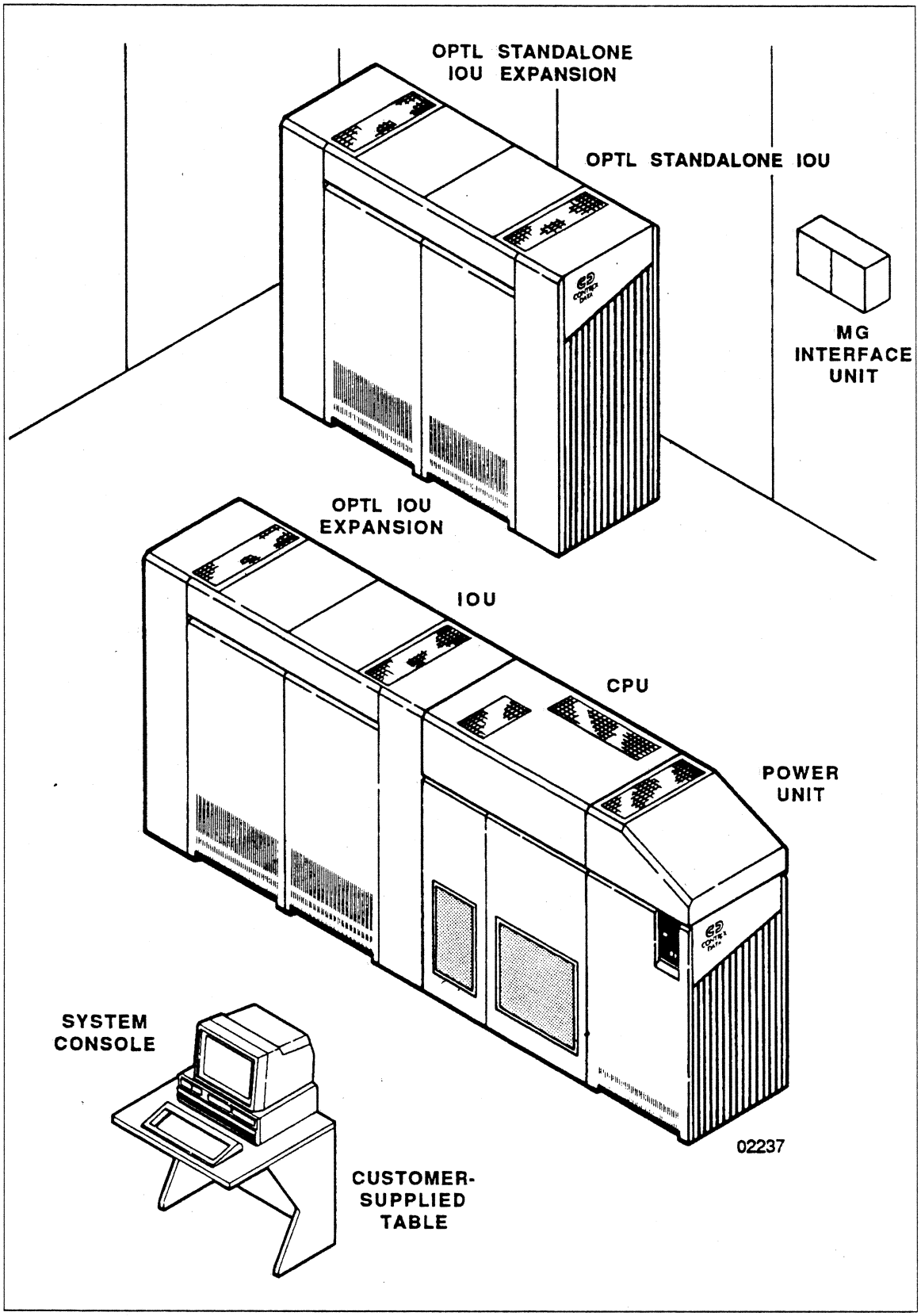

Figure 1-5. IOU Configurations

CYBER 960 IOU Functional Characteristics

The CYBER 960 IOU has the following functional characteristics.

- An NIO subsystem consisting of 20 CYBER 170 compatible PPs; each PP has an 8K x 16-bit word independent peripheral processor memory (PPM) degradeable to 4K x 16 bits (refer to the CIP Reference Manual listed under Additional Related Manuals in About This Manual for information on degrading PPMs)
- Execution of 12- or 16-bit PP code
- Operating speed at 250 ns and a minor cycle at 50 ns
- Port to CM
- 24 CYBER 170 compatible I/O channels available
- Interface to real-time clock, radial interface, and two-port multiplexer
- Bounds register controlling write access to CM
- SECDED data verification on all PPMs
- Parity checking on all major data and address paths
- Maintenance channels giving PPs access to CP, CM, and IOU registers to perform system initialization and maintenance functions; the maintenance channel of standalone IOU in a dual-IOU option has access to only IOU registers

CYBER 962 IOU and IOU Options Functional Characteristics

The CYBER 962 IOU and the optional IOUs have the following functional characteristics.

- A CIO subsystem consisting of 5 or 10 PPs. Each PP has an 8 K x 16-bit PPM. In addition, an optional DMA-enhanced ISI channel adapter, an optional CYBER 170 DMA channel adapter, and an optional DMA IPI channel adapter support DMA transfer between CM and an external device as well as standard I/O data transfer. An adapter can be installed in any one of ten channel locations in the CIO cabinet. There are two types of CYBER 170 DMA transfers, fast and normal. Fast transfers are used with the Extended Semiconductor Memory-II (ESM-II), and normal transfers are used with other CYBER 170 external devices.
- Execution of 16-bit PP code
- Operating speed of 250 ns and a minor cycle at 50 ns
- Port to CM
- Interface to real-time clock, radial interface, and two-port multiplexer
- SECDED data verification on all PPMs
- Parity checking on all major data paths
- Maintenance channels giving PPs access to CP, CM, and IOU registers to perform system initialization and maintenance functions
- A CIO subsystem consisting of 10, 15, or 20 PPs, each with an 8K x 16-bit PPM
- 18 concurrent DMA channels, which may be any combination of the following.
  - ISI channels (maximum transfer rate of 12M bytes/s)
  - IPI channels (maximum transfer rate of 10M bytes/s)
  - CYBER 170 channels (maximum transfer rate of 3M bytes/s)

Major System Component Descriptions

The following are the major system components.

- Power unit
- The CPU which includes the CP, CM, and CMC
- IOU and optional IOUs
- System console

Brief descriptions of these components are provided in the remainder of this chapter. The descriptions are in reference to the computer system block diagram shown in figure 1-6.

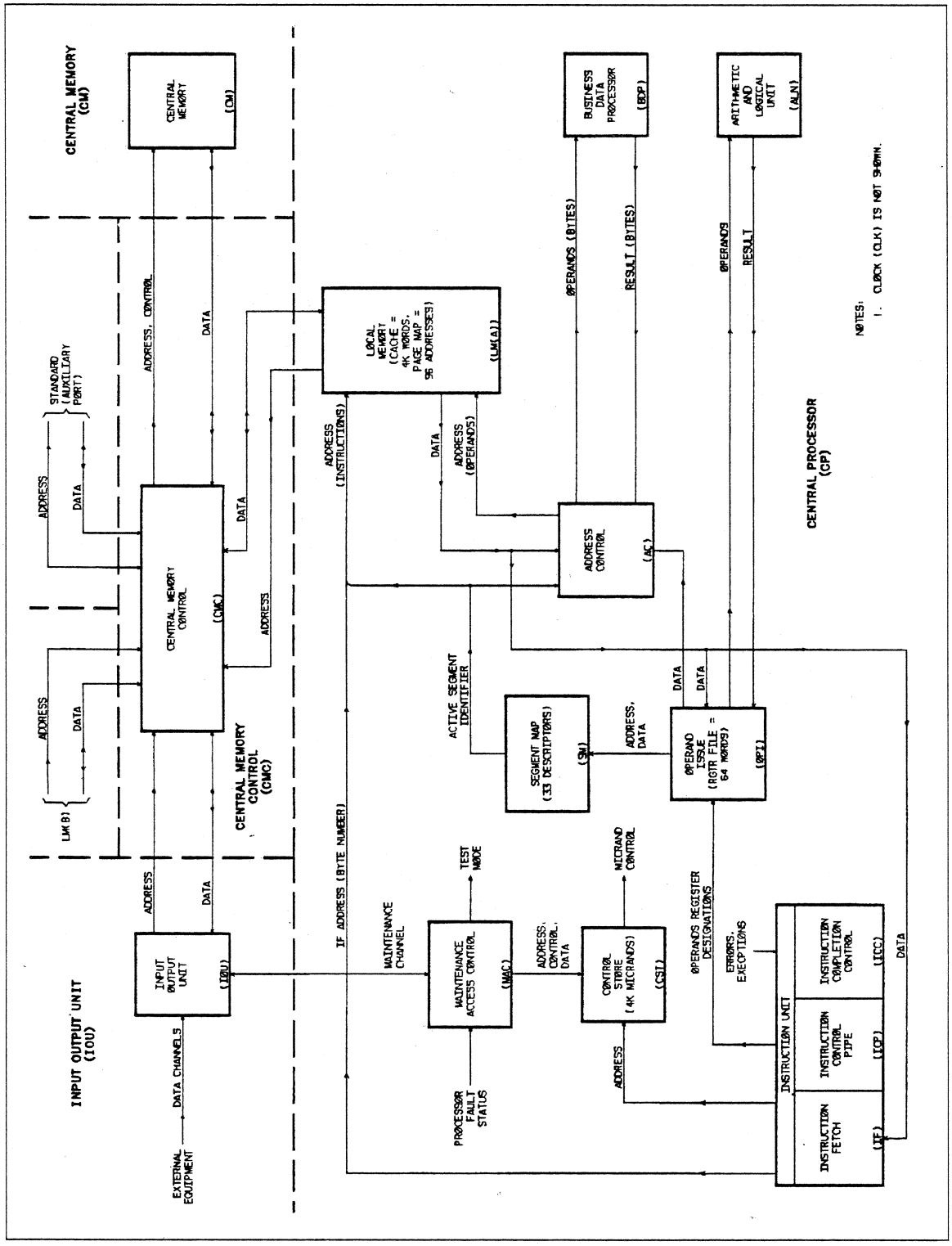

Figure 1-6. CYBER 960/962 System Block Diagram

Power Unit

The power unit is part of the power subsystem of the computer system. It performs the following tasks.

- Provides on/off control
- Generates warnings, such as when the temperature limits are exceeded, blower faults are detected, or a motor generator status line drops
- Contains power supplies that assist in converting 400-Hz power into computer logic DC voltage
- Supplies power to the blowers which are part of the cooling system for each cabinet in the computer system

Refer to the Mainframe Power and Environmental Subsystem Hardware Maintenance Manual listed in the hardware manual set figure in Related Manuals for more information about the power unit.

Central Processing Unit (CPU)

The CPU consists of the CP, CM, and CMC, which are discussed in the following paragraphs.

Central Processor

The CP consists of the following.

- Instruction section
- Operand issue section
- Arithmetic section
- Segment map
- Local memory
- Addressing section
- Business data processing (BDP) section
- Maintenance access control (MAC)

The CP is isolated from the IOU and is thus able to carry on computation or character manipulation unencumbered by I/O requirements.

Instruction Section

The instruction section directs the arithmetic and manipulative functions for instruction execution. The instruction section functions include the following.

- Initializing registers, controls, and memories
- Storing, accessing, decoding, and initiating a microprogram which controls CP operation in both CYBER 170 State and Virtual State
- Prefetching and disassembling instructions from CM
- Initiating interrupts when an error or exception condition occurs while an instruction is executing

Operand Issue Section

The operand issue section contains the registers of the two CP register categories.

- Process state registers
- Processor state registers

These registers are located either in the 64-word register file or throughout the hardware as various "live" registers. The process state registers contain information related to the current process (job). This information includes operands and exchange package data required for instruction execution. These registers change as the processes switch.

The 64-word register file contains the operating registers for instructions. These are the A, B, and X registers for CYBER 170 State instructions, and the A and X registers for Virtual State instructions. Process state registers are described in detail in chapter 2.

The processor state registers contain information related to the system and the CP hardware. Processor state registers are described in detail in chapter 2.

Arithmetic Section

The arithmetic section consists of the arithmetic and logical network (ALN).

The ALN performs those operations that require logical processing, operand shifting, and FP and integer arithmetic.

The ALN operates on values supplied by the operand issue section, or in some cases, the BDP section. (The BDP section performs most BDP operations independently.) All results return to the operand issue section except for exception conditions, which are sent to the instruction section to initiate interrupt handling.

The ALN consists of a general network and a multiply/divide network. The general network:

- Adds and subtracts integers and FP coefficients
- Performs exponent arithmetic associated with all FP operations
- Performs Boolean, FP normalize, shift, and conditional-branch test functions

The multiply/divide network forms Virtual State integer products and FP product coefficients for both CYBER 170 State and Virtual State.

Segment Map

Segment map contains the hardware to convert PVAs to SVAs. Conversion is accomplished by translating the user's segment number to an active segment identifier (ASID).

To reduce CM access time, segment map contains up to 32 of the most recently used 64-bit entries from the segment descriptor table (SDT) in CM. If the requested entry is not available, segment map obtains it from the SDT.

Segment map also performs all of the access validations for addressing memory. These include:

- Security ring tests
- Key and lock tests
- Read/write/execute privilege validity tests

Local Memory

The local memory contains the hardware to translate SVAs received from the segment map to real-memory addresses (RMAs). To reduce CM access time, local memory also contains two buffer memories: cache memory and page map.

- Cache memory contains 4096 words of the most recently used entries in the system virtual memory.
- Page map contains up to 96 of the most recently used page descriptors from the system page table (SPT).

For a data request, the CP simultaneously tests cache memory and page map memory to see if the requested SVA is present. If a cache memory hit occurs, the CP reads the requested data from cache memory.

If the data is not in cache, the system page table is required to convert an SVA to an RMA to access CM. The presence of the most recently used SPT entries in page map accelerates addressing of CM. The page map test, now relevant because the cache test was unsuccessful, searches the SPT for the requested page descriptor. If the test is unsuccessful, the CP retrieves the page with the requested data from CM.

Addressing Section

The addressing section performs the following functions.

- Forms the byte number of addresses sent to local memory for register file data or BDP stream data
- Provides assembly and disassembly data paths and control for data streams from local memory to the BDP section, and vice versa
- Processes the load and store bit, byte, and word instructions
- Processes the addresses for multiword memory to/from register transfers

Business Data Processing (BDP) Section

This performs BDP operations on 12 types of binary, alphanumeric, and decimal data. Although the BDP section performs most BDP operations independently, for some operations it may require processing assistance from the ALN in the execution section.

Maintenance Access Control (MAC)

The MAC performs initialization and maintenance operations in the CP. These operations, controlled by the system console through the IOU, include the following.

- Initialize registers, controls, and memories
- Communicate CP error/status information to the IOU when requested by a PP
- Read and write CP-resident registers and memories
- Clock initialization and tuning
- Reconfigure hardware
- Starting and stopping CP execution

The IOU sends codes to MAC to indicate the operations to be performed and the affected memory device, registers, and addresses.

Central Memory

The CYBER 960 and 962 CM (figure 1-6) organizes DRAM into eight independent banks.

Memory data words comprise 64 data bits plus 8 SECDED bits. The SECDED bits allow CMC to correct single-bit failures and detect double-bit failures during a read operation before sending the data to the requesting unit. For all failures, the CP logs the error and system software determines corrective action.

Central Memory Control (CMC)

CMC controls the flow of data between CM and the requesting system components through multiple ports and resolves port conflicts. The CMC contains a distributor which multiplexes data from ports to CM. The distributor includes the error-correction-code (ECC) generator, SECDED logic, and partial-write logic.

The CMC ports allow access to CM from:

- CP-0
- CP-1 (second CP)
- IOU
- Other external processing devices

Input/Output Unit

The CYBER 960 basic IOU is nonconcurrent, while the CYBER 962 basic IOU is concurrent. Both the CYBER 960 and 962 have the following IOU options available.

- IOU expansion
- Standalone IOU
- Standalone IOU expansion

Each of these options is functionally identical and is a subset of the concurrent CYBER 962 basic IOU. They are distinguished only by their position relative to the CPU. Figure 1-5 shows the maximum IOU configuration.

CYBER 960 IOU

The CYBER 960 IOU consists of the following.

- 20 logically independent NIO PPs
- 23 CYBER 170 channel interfaces
- Real-time clock interface (channel 14_8)
- Two-port multiplexer interface (channel 15_8)
- Maintenance channel interface (channel 17_8)
- Cache invalidation available on all CM writes except Read and Set Lock and Read and Clear Lock instructions
- Interface to CM
- OS Bounds register to limit writes to CM

The PPs are organized in groups of five, called barrels. The PPs in a barrel time-share common hardware. Each PP has its own 4K or 8K independent memory and communicates with all I/O channels and with CM.

CYBER 962 IOU and IOU Options

The basic 962 IOU and the IOU options consists of the following.

- Ten logically independent CIO PPs with eight DMA channels
- Five independent CIO PPs with five channels (each optional add on)
- DMA channel each containing ISI, IPI, or CYBER 170 channel protocol
- Small computer system interface (SCSI) (channels 32_8 and 33_8)
- Maintenance channel interface (radial) (channel 17_8)
- Real-time clock interface (channel 14_8)
- Two-port multiplexer interface (channel 15_8)
- Internal communication interface (channels 0, 1_8, 12_8, and 13_8)
- One port to CM

The PPs are organized in groups of five, called barrels. The PPs in a barrel time-share common hardware. Each PP has its own 8K independent memory and communicates with designated I/O channels and with CM.

System Console

Two different system consoles are available for two-way communication between the system and the computer operator and/or maintenance personnel, either locally or remotely located. Both systems run the MS-DOS operating system. They are equipped with a alphanumeric keyboard, a 40M- or 91M-byte large disk memory, a 5.25-in flexible disk drive, and a color monitor. They also contain nine RS-232-C communication ports and a parallel printer port.

The 19003-2 system console, required by all CYBER 962 systems, contains a dedicated load device (DLD) which uses a 91M-byte hard disk drive. The 19003-1 system console uses a 40M-byte hard disk drive. The 19003-1 system console is required on all CYBER 960 systems that contain an expansion IOU. Both system consoles connect to the IOU through the two-port multiplexer. The DLD of the 19003-2 system console uses SCSI on channels 32_8 and 33_8.

The alphanumeric keyboard and the monitor screens enable the computer operator to perform normal operator duties, system initialization, diagnostic sequences, and allow the console to be switched into remote mode of operation for off-site status analysis, maintenance actions, and troubleshooting. Detailed descriptions of system console operations appear in the System Console Operations/Maintenance Guide shown in the hardware manual set figure under Related Manuals.

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Functional Descriptions 2

This chapter describes:

- Central processor (CP) operating states
- Environment interface (EI)
- Intrastate modes of operation
- Dual-CP operation
- Functional descriptions of the CP, central memory (CM), central memory control (CMC) and input/output unit (IOU)

Central Processor (CP) Operating States

The CYBER 960 CP supports two states of operation: Virtual State and CYBER 170 State; the CYBER 962 CP supports only Virtual State.

Virtual State uses the Virtual State instruction set and data formats. CYBER 170 State uses the CYBER 170 State CP instruction set and data formats.

Although Virtual State is the native operating state of the system, both environments may be present at the same time in the CYBER 960 system. However, the CP executes in one or the other environment.

Portions of Virtual State support and track CYBER 170 State operation. However, Virtual State is transparent to the CYBER 170 State operating system and any user jobs executing in the CYBER 170 State environment.

Environment Interface (EI)

EI is a Virtual State operating system routine that provides the interface between CYBER 170 State and Virtual State needed for the CYBER 960 system. EI directly supports the CYBER 170 State environment by simulating those portions of that environment not provided by the CP hardware.

The basic EI tasks are to:

- Support system initialization and deadstart of the CYBER 170 State environment
- Simulate CYBER 170 State hardware and software error processing
- Simulate certain CYBER 170 State instructions unimplemented by the CP hardware
- Process Virtual State errors occurring in CYBER 170 State

Refer to Intrastate Modes of Operation, following, for additional information on Virtual State EI operations.

Intrastate Modes of Operation

Virtual State and CYBER 170 State each have two modes of execution: job mode and monitor mode.

- Job mode executes programmed sequences of instructions (jobs) in the CP.
- Monitor mode executes various operating system routines (for example, job sequencer, trap handler, and memory manager) which control the loading, scheduling, executing, and outputting of user jobs. The monitor mode routines are always available to the CP when it requests any type of monitor mode intervention.

The CYBER 170 State environment exists within Virtual State job mode. The operating system supports this environment somewhat like a special-purpose Virtual State job.

CYBER 170 State has the characteristics of CYBER 170 computer system CPs. For detailed information on CYBER 170 State, refer to the CYBER 170 State Hardware Reference Manual listed under Related Manuals.

The CYBER 960 CP always operates in one of the following environments.

- Virtual State job mode
- Virtual State monitor mode
- CYBER 170 State job mode
- CYBER 170 State monitor mode

These four environments, plus specific EI operations, are briefly described in the following paragraphs. Figure 2-1 shows the interaction among operating states, intrastate modes of operation, and EI.

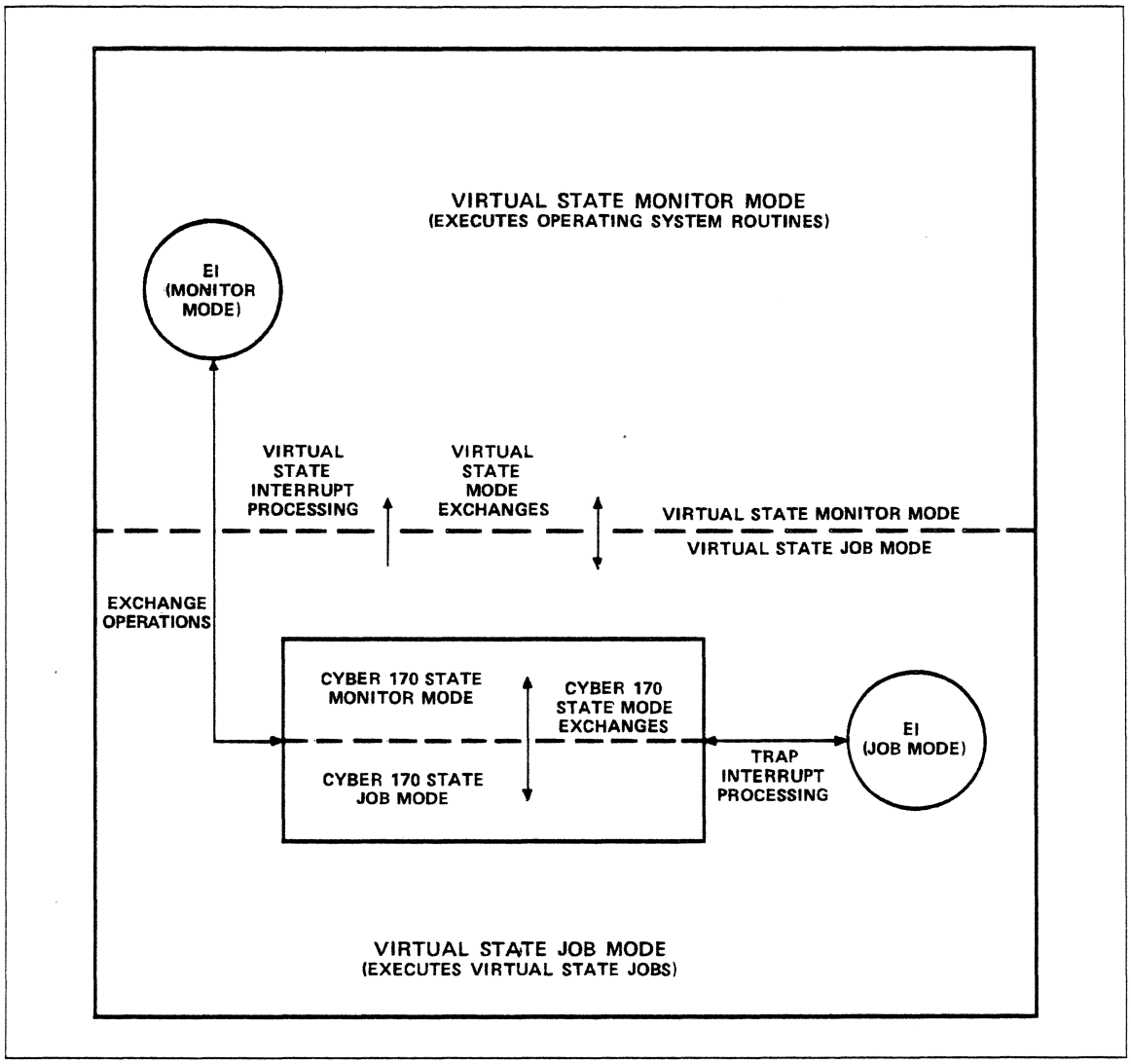


Figure 2-1. Operating States Interaction

Virtual State Job and Monitor Modes

Virtual State modes execute NOS/VE jobs, interstate exchange instructions, and programs transferred from CYBER 170 State to Virtual State.

Virtual State Job Mode

Virtual State job mode executes programmed sequences of Virtual State instructions in the CP. While in Virtual State job mode, an exchange interrupt or an exchange instruction causes an exchange to Virtual State monitor mode.

Virtual State Monitor Mode

Virtual State monitor mode executes operating system routines that perform Virtual State monitor activities. This mode performs the following tasks.

- Exchange and trap interrupt processing
- Simulates certain CYBER 170 State instructions
- Executes restricted CP instructions
- Processes hardware and software errors detected in both Virtual State and CYBER 170 State

EI Operations in Virtual State

EI operations occur in both Virtual State job and monitor modes. The primary EI job mode task is to perform CYBER 170 State interrupt processing, which comprises the following.

- Simulating CYBER 170 State error exit conditions
- Trapping from CYBER 170 State to routines in Virtual State job mode that:
  - Execute CYBER 170 State compare/move instructions
  - Purge cache memory for memory word blocks in CM and unified extended memory (UEM)
  - Ready the CP for transition from Virtual State to CYBER 170 State
  - Transfer blocks of CM or UEM words either within the CYBER 170 State environment or between operating states

The primary EI monitor mode task is to perform exchange operations within CYBER 170 State if hardware or software errors are detected in CYBER 170 State job or monitor mode.

CYBER 170 State Job and Monitor Modes

CYBER 170 State job and monitor modes exist within Virtual State job mode.

- CYBER 170 State job mode executes programmed sequences of CYBER 170 State instructions in the CP.
- CYBER 170 State monitor mode executes operating system routines that perform CYBER 170 State monitor activities.

Mode Switching Within CYBER 170 State

Within CYBER 170 State, switching between monitor mode and job mode as shown in the following text does not require an exchange to Virtual State monitor mode.

Switch	Cause
Job-to-monitor	• PP-directed CYBER 170 State exchange request • CYBER 170 State exchange jump instruction • Hardware or conditional software error
Monitor-to-job	CYBER 170 State exchange jump instruction

Transferring from CYBER 170 State to Virtual State

The following CP conditions cause a transfer (trap or exchange) to Virtual State from CYBER 170 State monitor or job mode.

- Explicit trap instruction (trap)
- Request for compare/move instruction (trap)
- Conditional software error in CYBER 170 State monitor mode (exchange)
- Illegal instruction in CYBER 170 State monitor mode (exchange)
- Virtual State errors detected in CYBER 170 State monitor or job mode (exchange)

Refer to Exception Handling in CYBER 170 State in Virtual State Hardware Reference Manual Volume 2, listed under Related Manuals in About This Manual, for further information.

Central Processor (CP)

The CP consists of:

- Instruction section
- Operand issue section
- Execution section
- Segment map
- Local memory
- Addressing section
- Business data processing (BDP) section
- Maintenance access control (MAC)

Instruction Section

The instruction section consists of logic for instruction lookahead, decode, and initiation.

The CYBER 960 instruction section implements the CYBER 170 State and Virtual State instruction sets by initiating microprogram sequences that obtain instruction operands and provide the control signals for execution.

The CYBER 962 instruction section implements Virtual State instruction sets only.

The instruction section also performs CP interrupt handling by initiating an interrupt handling routine when an error or exception condition occurs while an instruction is executing.

Instruction Lookahead

The instruction lookahead hardware speeds up instruction processing by stacking prefetched instructions to make them immediately available for execution.

It also assumes program branches to be taken, and fetches and issues instructions along that path before the CP determines the actual branch outcome.

Instruction Prefetch

To maintain a continuous flow of instructions, the instruction section prefetches a maximum of 12 instructions from local memory to make the next instruction immediately available when the previous instruction completes execution. This occurs by reading instructions from cache/CM into a series of buffer ranks.

Branch Assumption

When the instruction section detects a conditional branch, it assumes that the branch condition will be met. It computes the branch target address and reads instructions from cache/CM starting at the target address.

If the branch is taken, the buffer ranks contain the next executable instruction words.

If the branch is not taken, the hardware purges the buffer ranks and resumes prefetching at the instruction word following the unsatisfied branch instruction. (In CYBER 170 State, this instruction word is located at a word boundary, while this may or may not be the case in Virtual State.)

Instruction Decode and Initiation

In both Virtual State and CYBER 170 State, instruction words read from CM contain from two to four instructions combined in a parcel arrangement. The instruction section decodes the CM instruction word into its separate instructions and issues control information to other functional units in the execution section to initiate instruction execution.

In CYBER 170 State, a two-parcel instruction is not permitted to cross a word boundary, while it is permitted in Virtual State. During Virtual State BDP operations, one or two two-parcel BDP descriptors follow the instruction parcels through execution.

Interrupt Handling

The instruction section can initiate an interrupt handling routine when an error or exception condition occurs while an instruction is executing. The error/exception conditions are a combination of stackable or unstackable conditions, allowing the instruction section to interrupt selectively.

The error and exception conditions accumulate in the monitor and user condition registers (refer to the description under Operand Issue Section). The instruction section examines the error/exception inputs to determine the type of interrupt. It then addresses the appropriate interrupt handling routine in monitor mode.

Operand Issue Section

The operand issue section consists of the process state and processor state registers, which are located in the 64-word register file or throughout the CP hardware as various live registers.

The 64-word register file contains the operating registers for CYBER 170 State and Virtual State instructions. The operating registers are:

- A, B, and X for CYBER 170 State
- A and X for Virtual State

The register file also holds other exchange package information and provides holding registers for intermediate results.

The live registers contain control information for various CYBER 170 State and Virtual State CP operations. The CP uses the constant output of the live registers during online operations. The live registers give the CP access to exchange package information which otherwise would have to be obtained from the register file.

Some of the live registers are writable under microprogram control but copies which are maintained in the register file may also be read. These registers typically contain control information rather than data. Normally they are loaded from an exchange package at the same time that exchange package enters the register file from central memory.

Other live registers are read-only registers under microprogram control. The contents of these registers change as a result of changes in the CP hardware environment. These changes typically impact system operation and require monitoring.

All register-file registers and live registers are either process state or processor state registers.

This distinction arises because the state of the process and the state of the processor characterize CP operation. The contents of the process state registers can be written into memory as a Virtual State exchange package for either a Virtual State process or a CYBER 170 State process. Figures 2-2 and 2-3 show the respective exchange packages. For detailed information on exchange packages and state switching operations, refer to volume 2 of this manual (listed under Related Manuals in About This Manual).

The principal registers of each category are described in the following paragraphs. For detailed functional descriptions of the remaining registers, refer to CP Registers in volume 2, chapter 2.

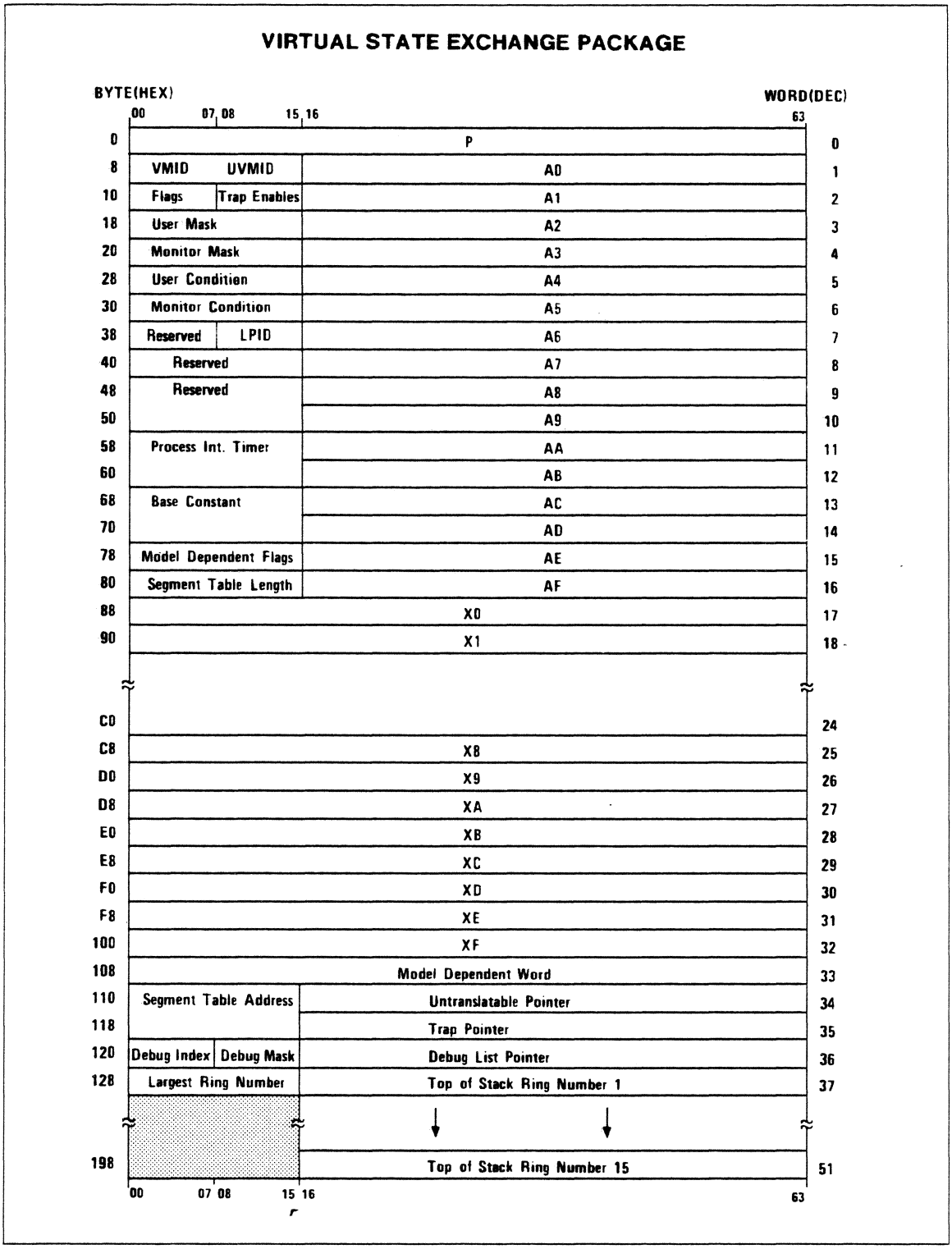
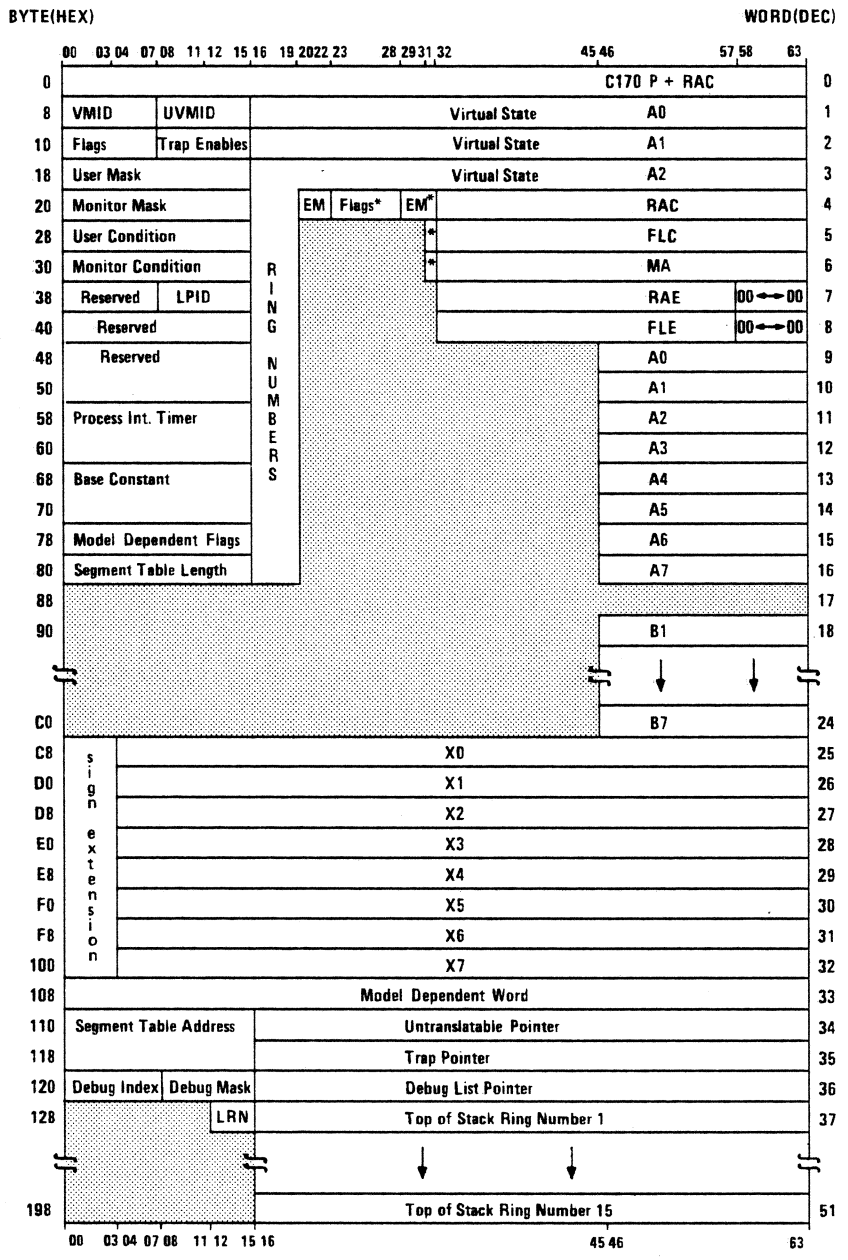

VIRTUAL STATE EXCHANGE PACKAGE
BYTE(HEX)
WORD(DEC)
00 07 08 15 16 63
0 P 0
8 VMID UVMID A0 1
10 Flags Trap Enables A1 2
18 User Mask A2 3
20 Monitor Mask A3 4
28 User Condition A4 5
30 Monitor Condition A5 6
38 Reserved LPID A6 7
40 Reserved A7 8
48 Reserved A8 9
50 A9 10
58 Process Int. Timer AA 11
60 AB 12
68 Base Constant AC 13
70 AD 14
78 Model Dependent Flags AE 15
80 Segment Table Length AF 16
88 X0 17
90 X1 18
C0 24
C8 X8 25
D0 X9 26
D8 XA 27
E0 XB 28
E8 XC 29
F0 XD 30
F8 XE 31
100 XF 32
108 Model Dependent Word 33
110 Segment Table Address Untranslatable Pointer 34
118 Trap Pointer 35
120 Debug Index Debug Mask Debug List Pointer 36
128 Largest Ring Number Top of Stack Ring Number 1 37
198 Top of Stack Ring Number 15 51
00 07 08 15 16 63

Figure 2-2. Virtual State Exchange Package



* Flags:

Bit 23, Word 4	UEM Enable Flag
Bit 24, Word 4	Expanded Addressing Select Flag (ESM Mode Flag)
Bit 25, Word 4	Extended Block Copy Flag
Bit 26, Word 4	Software Flag
Bit 27, Word 4	Instruction Stack Purge Flag
Bit 28, Word 4	Software Flag
Bit 29, Word 4	EM-Indefinite Operand
Bit 30, Word 4	EM-Infinite Operand
Bit 31, Word 4	EM-Address out of Range
Bit 31, Word 5	C170 Monitor Flag
Bit 31, Word 6	Exit Mode Halt

Figure 2-3. Intrastate Exchange Package

Process State Registers

The process state registers relate to a specific Virtual State process executing in the CP. Various process state registers in the CYBER 960 also support CYBER 170 State operation. The exchange package for each process contains the step-by-step operating register contents as directed by that process' execution. In addition, the exchange package holds other detailed process state information such that the CP may dynamically switch between exchange packages (that is, processes) while preserving process integrity.

When a process executes in the CP, its exchange package resides in the process state registers. When a process awaits execution, its exchange package resides in CM. The process state registers include the following.

- Operating registers
  - Sixteen 48-bit address (A) registers, A0 through AF
  - Sixteen 64-bit operand (X) registers, X0 through XF
- Interrupt-handling registers (16 bits each)
  - Monitor condition register (MCR) and monitor mask register (MMR)
  - User condition register (UCR) and user mask register (UMR)

Refer to table 2-1 for a complete list of the process state registers. The principle process state registers are described in this chapter. The remaining process state registers are described under CP Registers in volume 2 of this manual (listed under Related Manuals in About This Manual).

Table 2-1. Process State Registers

Register or Flag Name	Number of Bits
Address (A0–AF) (16 registers)	48
Base constant (BC)	32
Debug index (DI)	6
Debug list pointer (DLP)	48
Debug mask (DM)	7
Critical frame flag (CFF)	1
On condition flag (OCF)	1
Process not damaged (PND)	1
Largest ring number (LRN)	4
Last processor identification (LPID)	8
Monitor condition register (MCR)	16
Monitor mask (MM)	16
Operand (X0–XF) (16 registers)	64
Process interval timer (PIT)	32
Program (P) address	64
Segment table address (STA)	32
Segment table length (STL)	12
Top-of-stack (TOS) pointer (15 registers)	48
Trap enables (TE)	2
Trap pointer (TP)	48
Untranslatable pointer (UTP)	48
Untranslatable virtual machine identifier (UVMID)	4
User condition (UCR)	16
User mask (UM)	16
Virtual machine identifier (VMID)	4

Operating Registers

The operating registers consist of the address (A) and operand (X) registers, which minimize memory references for arithmetic operands and results.

The time an exchange package resides in CP hardware is called an instruction interval. During this interval, the operating register contents can be changed by CP instructions (the other process state registers change only as a result of an exchange jump, Copy-to-State-Register instruction, or Branch-on-Condition-Register instruction).

Address (A) Registers – The A registers are primarily CM operand address registers which contain process virtual addresses (PVAs).

Operand (X) Registers – The X registers are primarily data handling registers for computation. Depending on the operation, the registers contain a logical quantity, a signed binary integer, or a signed floating-point (FP) number. Operands and results transfer between CM and the X registers.

Interrupt Handling Registers

The condition registers (MCR and UCR) and associated mask registers (MMR and UMR) provide the CP interrupt structure. These registers detect interrupt conditions which cause any of the following CP responses.

Response	Description
Exchange	An exchange interrupt switches CP execution to a monitor mode interrupt handling routine after an intermode exchange occurs. An exchange can only be caused by an interrupt condition occurring in job mode. Monitor (system) conditions cause nearly all exchange interrupts; exceptions are user (process) conditions that occur with traps disabled.
Halt	The CP halts and the IOU takes steps to resolve the problem.
Stack	The CP records the condition but temporarily defers processing of the interrupt.
Trap	A trap interrupt switches CP execution to another section of code in the same address space as the executing process. It does not cause an exchange of processes, and may occur in both job and monitor modes. A trap triggers from the occurrence of a certain process interrupt condition. The trapped-to code executes a specific routine that resolves the interrupt and returns control to the process.

These responses to MCR and UCR interrupts depend on whether traps are enabled or disabled, the state of the mask registers, and what the current operating mode is when the interrupt occurs.

The CP usually runs with traps enabled. Traps are disabled, however, to keep traps from occurring when certain sections of code are executing.

- In monitor mode, traps are disabled to prevent interrupts caused by the operating system or peripheral devices.
- In job mode, traps are disabled to prevent trap interrupts from interrupting the execution of job mode trap handling routines. (However, exchanges caused by monitor conditions can interrupt these trap handling routines if traps are disabled.)

CP interrupt responses characteristic of the operating mode are described in the following subsections.

Monitor Condition Register (MCR) - The MCR provides the CP interrupt structure for interrupt conditions which must be serviced by monitor mode. The MCR contains 16 bits, each of which records a different interrupt condition in the CP. The MCR conditions are of higher priority (and are processed before) the UCR conditions.

The MCR conditions include:

- Addressing/security errors in CP or CM
- Hardware errors
- Major software errors
- Page faults

The specific MCR conditions and corresponding CP responses are listed in table 2-2 and described in detail under CP Interrupts in volume 2 of this manual (listed under Related Manuals in About This Manual).

An MCR bit set in job mode with traps enabled or disabled causes an exchange to a monitor mode to execute an interrupt handling routine. This routine analyzes the error and determines corrective action.

- An MCR bit set in monitor mode with traps enabled transfers control to a trap handling routine within monitor mode.
- An MCR bit set in monitor mode with traps disabled causes the CP to stack the condition or halt, depending on the condition.

Each bit in the MCR has an associated mask bit in the MMR. The 16 mask bits allow selective processing of MCR interrupts (refer to the following paragraphs).

Table 2-2. Types of Interrupts for Monitor Condition Register Bits[1]

Bit	Definition	Type A[2]	Type B[3]	Type C[4]	Type D[5]	Type E[6]	Instr[7]
48	Detected uncorrectable error	Exch	Trap	Exch	Halt	Halt	–
49	Unassigned	Exch	Trap	Exch	Halt	Halt	–
50	Short warning	Exch	Trap	Exch	Stack	Stack	P+
51	Instruction specification error	Exch	Trap	Exch	Halt	Halt	P
52	Address specification error	Exch	Trap	Exch	Halt	Halt	P
53	170 exchange request	Exch	Trap	Exch	Stack	Stack	P+
54	Access violation	Exch	Trap	Exch	Halt	Halt	P
55	Environment specification error	Exch	Trap	Exch	Halt	Halt	P

Notes:

1. This table lists interrupts applicable to both the MCR and MMR.

2. Occurs with trap enabled in job mode with associated MMR bit set.

3. Occurs with trap enabled in monitor mode with associated MMR bit set.

4. Occurs with trap disabled in job mode with associated MMR bit set.

5. Occurs with trap enabled in monitor mode with associated MMR bit set.

6. Occurs with trap enabled or disabled in either job or monitor mode with associated MMR bit clear.

7. Indicates the next instruction executed when program resumes.

(Continued)

Table 2-2. Types of Interrupts for Monitor Condition Register Bits[1] *(Continued)*

Bit	Definition	Type A[2]	Type B[3]	Type C[4]	Type D[5]	Type E[6]	Instr[7]
56	External interrupt	Exch	Trap	Exch	Stack	Stack	-
57	Page table search without find	Exch	Trap	Exch	Halt	Halt	-
58[8]	System call status	-	-	-	-	-	-
59	System interval timer	Exch	Trap	Exch	Stack	Stack	P+
60	Invalid segment or ring number 0	Exch	Trap	Exch	Halt	Halt	P/P+[9]
61	Outward call or inward return	Exch	Trap	Exch	Halt	Halt	P
62	Soft error log	Exch	Trap	Exch	Stack	Stack	P+
63[8]	Trap exception status	-	-	-	-	-	-

Notes:

1. This table lists interrupts applicable to both the MCR and MMR.

2. Occurs with trap enabled in job mode with associated MMR bit set.

3. Occurs with trap enabled in monitor mode with associated MMR bit set.

4. Occurs with trap disabled in job mode with associated MMR bit set.

5. Occurs with trap enabled in monitor mode with associated MMR bit set.

6. Occurs with trap enabled or disabled in either job or monitor mode with associated MMR bit clear.

7. Indicates the next instruction executed when program resumes.

8. This bit is a flag only and does not cause any hardware action.

9. Instruction is P except for Ring O loads when it is P+.

Monitor Mask Register (MMR) – The MMR contains 16 bits, each of which is a mask bit associated with a specific MCR condition. The mask bits control interrupt response when a corresponding MCR bit sets. At certain times during program execution, it may be necessary to defer processing of specific MCR conditions. For example, when executing in CYBER 170 State, the CYBER 170 State exchange request (MCR bit 53) should not be processed and stacks until execution of the previous CYBER 170 State process terminates.

All MMR bits are set if no masking of interrupts is desired. Clearing an MMR bit masks its corresponding interrupt condition in the MCR. The CP Copy-to-State-Register instructions are used to set/clear specific MMR bits (refer to volume 2 listed under Related Manuals in About This Manual).

The MCR is normally all zeros. An interrupt condition sets the appropriate MCR bit. The CP performs a logical product (AND) of the 16 MCR and MMR bits (figure 2-4). If the corresponding MMR bit is set (unmasked), an interrupt occurs. If the corresponding MMR bit is clear (masked), the CP either halts or stacks the condition and processes the interrupt later when the mask bit sets.

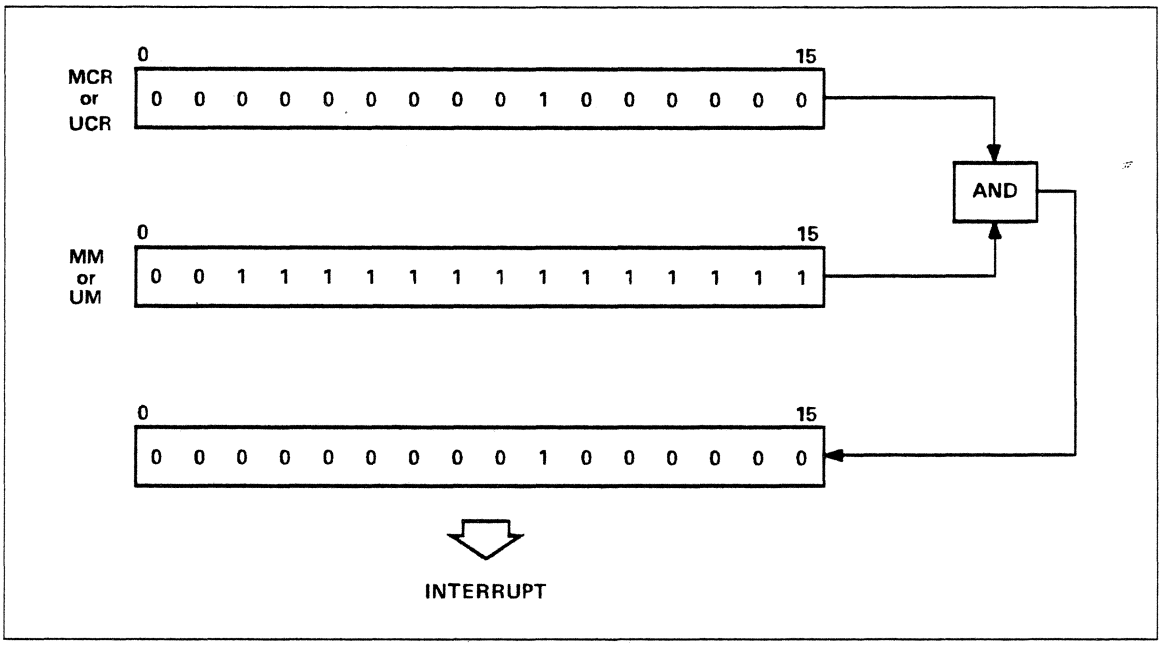


Figure 2-4. MCR and UCR Interrupt Mechanism

User Condition Register (UCR) – The UCR provides the CP interrupt structure for conditions which relate primarily to instruction execution, and which do not require monitor mode intervention. The UCR contains 16 bits which, like the MCR, record different interrupt conditions in the CP. The UCR conditions include:

- Execution errors
- Arithmetic errors
- Invalid data
- Invalid instructions

A UCR bit set in job or monitor mode with traps enabled causes a trap to a trap handling routine within the address space of the process. A UCR bit set in job or monitor mode with traps disabled generally causes the CP to stack the condition. For the monitor conditions grouped within the UCR, an interrupt in job mode causes an exchange to monitor mode to execute an interrupt handling routine, and an interrupt in monitor mode halts the CP.

Each bit in the UCR has an associated mask bit in the UMR. The 16 mask bits allow selective processing of UCR interrupts (refer to the following paragraphs).

The specific UCR conditions are listed in table 2-3 and described in detail under CP Interrupts in volume 2, listed under Related Manuals in About This Manual.

User Mask Register (UMR) – The UMR contains 16 bits which, like the MMR, are mask bits associated with specific UCR conditions. The mask bits control interrupt action when a corresponding UCR bit sets. (At certain times during program execution, it may be necessary or desirable to defer processing of specific UCR conditions. For example, when testing and debugging a new program, it may be desirable to disable interrupts caused by out-of-range arithmetic results, UCR bit 57.)

All UMR bits are set if no masking of interrupts is desired. Clearing a UMR bit masks its corresponding interrupt condition in the UCR. The CP copy instruction is used to set/clear specific UMR bits. Refer to CP Copy Instructions in volume 2 of this manual (listed under Related Manuals in About This Manual).

The UCR is normally all zeros. An interrupt condition sets the appropriate UCR bit. The CP performs a logical product (AND) of the 16 UCR and UMR bits (refer to figure 2-4). If the corresponding UMR bit is set (unmasked), an interrupt occurs. If the UMR bit is clear (masked), the CP stacks the condition and processes the interrupt later when the mask bit sets. However, as shown in table 2-3, certain UCR conditions require direct attention and cannot be masked.

Table 2-3. Types of Interrupts for User Condition Register Bits[1]

Bit	Definition	Type A[2]	Type B[3]	Type C[4]	Type D[5]	Type E[6]	Instr[7]
48	Privileged instruction fault	Trap	Trap	Exch	Halt	Note[8]	P
49	Unimplemented instruction	Trap	Trap	Exch	Halt	Note[8]	P
50	Free flag	Trap	Trap	Stack	Stack	Note[8]	P
51	Process interval timer	Trap	Trap	Stack	Stack	Note[8]	P+
52	Inter-ring pop	Trap	Trap	Exch	Halt	Note[8]	P
53	Critical frame flag	Trap	Trap	Exch	Halt	Note[8]	P
54	Unassigned	-	-	-	-	-	-
55	Divide fault	Trap	Trap	Stack	Stack	Stack	P
56	Debug	Trap	Trap	Stack	Stack	Stack	P
57	Arithmetic overflow	Trap	Trap	Stack	Stack	Stack	P

Notes:

1. This table lists interrupts applicable to both the UCR and UMR.

2. Occurs with trap enabled in job mode with associated UMR bit set.

3. Occurs with trap enabled in monitor mode with associated UMR bit set.

4. Occurs with trap disabled in job mode with associated UMR bit set.

5. Occurs with trap enabled in monitor mode with associated UMR bit set.

6. Occurs with trap enabled or disabled in either job or monitor mode with associated UMR bit clear.

7. Indicates the next instruction executed when program resumes.

8. This is permanently set.

(Continued)

Table 2-3. Types of Interrupts for User Condition Register Bits[1] *(Continued)*

Bit	Definition	Type A[2]	Type B[3]	Type C[4]	Type D[5]	Type E[6]	Instr[7]
58	Exponent overflow	Trap	Trap	Stack	Stack	Stack	P+
59	Exponent underflow	Trap	Trap	Stack	Stack	Stack	P+
60	FP loss of significance	Trap	Trap	Stack	Stack	Stack	P+
61	FP indefinite	Trap	Trap	Stack	Stack	Stack	P
62	Arithmetic loss of significance	Trap	Trap	Stack	Stack	Stack	P
63	Invalid BDP data	Trap	Trap	Stack	Stack	Stack	P

Notes:

1. This table lists interrupts applicable to both the UCR and UMR.

2. Occurs with trap enabled in job mode with associated UMR bit set.

3. Occurs with trap enabled in monitor mode with associated UMR bit set.

4. Occurs with trap disabled in job mode with associated UMR bit set.

5. Occurs with trap enabled in monitor mode with associated UMR bit set.

6. Occurs with trap enabled or disabled in either job or monitor mode with associated UMR bit clear.

7. Indicates the next instruction executed when program resumes.

Processor State Registers

The processor state registers contain information about the state of the CP hardware, rather than a unique process. This group of registers comprises maintenance registers and other various processor state registers (table 2-4).

The maintenance registers provide information about the condition of CP hardware. In some cases, they can be set to force faults in the CP to verify the integrity of the fault detection hardware. The other processor state registers contain pointers/parameters of tables and exchange packages in CM. All processor state registers are accessible to the CP and PPs. These registers change only as a result of an exchange jump, if at all. Some may also change under monitor mode control.

The principal processor state registers are described in this chapter. The remaining processor state registers are described under CP Registers in volume 2 of this manual (listed under Related Manuals in About This Manual).

Table 2-4. Processor State Registers

Register Name	Number of Bits
Dependent Environment Control (DEC)	32
Element Identification (EI)	32
Job Process State (JPS)	32
Model-Dependent Word (MDW)[1]	64
Monitor Process State (MPS)	32
Options Installed (OI)	64
Page Size Mask (PSM)	7
Page Table Address (PTA)	32
Page Table Length (PTL)	14
Processor Fault Status (PFS)	352
Processor Identification (PI)	8
Processor Test Mode (PTM)	48
Status Summary (SS)	6
System Interval Timer (SIT)	32
Virtual Machine Capability List (VMCL)	16

Note:

1. MDW is used as the Keypoint Buffer Pointer.

Job Process State (JPS) Register

The JPS register holds the real-memory address of the first entry in an exchange package in CM. This address indicates where a job's process state registers are:

- Stored in CM in a job-to-monitor mode exchange
- Retrieved from CM in a monitor-to-job mode exchange

The JPS register works in tandem with the Monitor Process State (MPS) register in a Virtual State exchange operation. In an exchange from monitor mode to job mode, the CP stores the environment of the monitor mode process in an exchange package at MPS (figure 2-5). The CP then initiates the process whose exchange package is located at JPS. This monitor-to-job mode exchange is initiated by an exchange instruction from within the monitor mode process.

In an exchange from job mode to monitor mode, the CP stores the environment of the job mode process in an exchange package at JPS (figure 2-6). The CP then initiates the process whose exchange package is located at MPS. This job-to-monitor mode exchange is initiated either from an exchange instruction or the occurrence of some interrupt condition requiring monitor mode intervention.

Monitor Process State (MPS) Register

The MPS register holds the real-memory address that points to the first entry in an exchange package in CM. This address indicates the source of a job's process state registers.

- Stored in CM in a monitor-to-job mode exchange
- Retrieved from CM in a job-to-monitor mode exchange

The MPS register works in tandem with the JPS register in a Virtual State exchange operation. Refer to Job Process State (JPS) Register and figure 2-5.

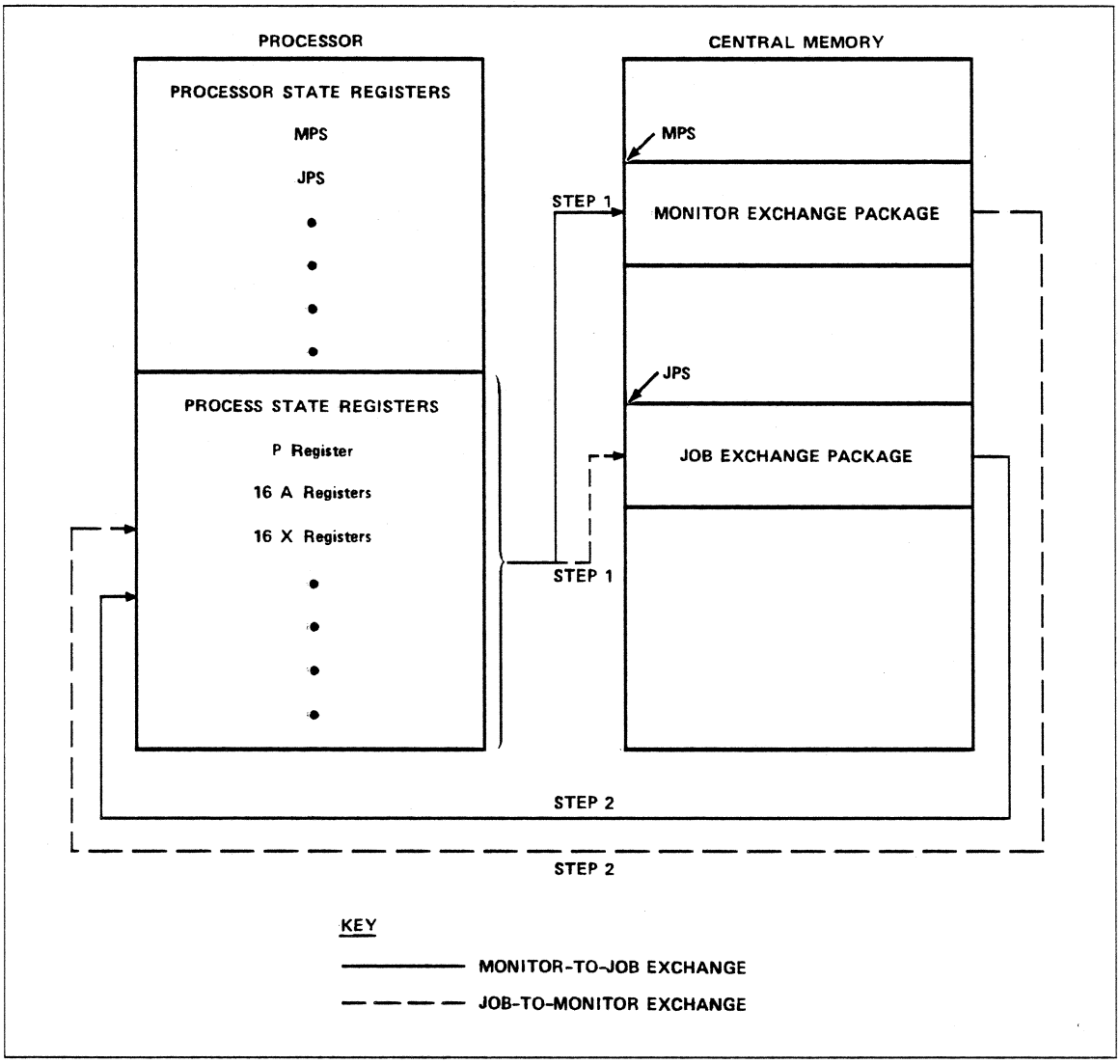


Figure 2-5. JPS and MPS Functions in Exchange Operation

Execution Section

The CP execution section consists of the arithmetic and logical network (ALN). The ALN contains hardware required to execute all FP and integer add, subtract, multiply, and divide instructions found in the CYBER 170 State and Virtual State instruction sets.

The ALN also processes CYBER 170 State and Virtual State shift and Boolean instructions, as well as CYBER 170 State pack/unpack, normalize, and population count instructions.

The ALN plays a role in branch instructions by evaluating branch conditions. It performs operations during most other CYBER 170 State and Virtual State instructions, passing operands between register file locations, comparing operands, or completing other required arithmetic steps.

The ALN performs operations on values supplied by the operand issue section or, in some cases, the BDP section. (The BDP section performs most BDP operations independently.) All results return to the operand issue section except for exception conditions, which are sent to the instruction section to initiate interrupt handling.

The ALN consists of a general network and a multiply/divide network as described in the following paragraphs.

General Network

The general network adds and subtracts integers and FP coefficients, and performs exponent arithmetic associated with all FP operations. Additionally, it performs Boolean, FP normalize, shift, and conditional branch test functions.

The integers are 18 or 60 bits in CYBER 170 State and 32 or 64 bits in Virtual State. FP operations use data in the form of:

- An exponent
- An exponent bias
- A 48-bit (single-precision) or 96-bit (double-precision) coefficient
- A coefficient bias

Negative CYBER 170 State operands typically are represented in ones-complement form, with negative Virtual State operands represented in twos-complement form. Operands may be 18 or 60 bits for CYBER 170 State operations, or 32 or 64 bits for Virtual State operations.

Multiply/Divide Network

The multiply/divide network performs Virtual State integer products and FP product coefficients for both CYBER 170 State and Virtual State.

In the former case, the product may be represented as a 32- or 64-bit Virtual State signed integer.

In the latter case, the product may be represented as a 48-bit signed coefficient (CYBER 170 State FP operations), or a 48- or 96-bit coefficient in signed magnitude form (Virtual State FP operations).

The network performs divide operations in which the coefficient of the dividend and divisor operands may be represented as a 32- or 64-bit signed integer (Virtual State only), or in one of the FP coefficient formats described in volume 2 of this manual (listed under Related Manuals in About This Manual).

Segment Map

Segment map contains the hardware to translate PVAs to SVAs. During this translation, the segment map also performs the security tests for addressing CM. To reduce CM access time, segment map contains up to 32 of the most recently used segment descriptors from the segment descriptor table.

Segment Map Address Translation

For the PVA-to-SVA translation, segment map obtains PVAs from A registers (for load and store instructions) and the P register (for addressing instructions).

Segment map performs the translation by changing the user's segment number to an active segment identifier (ASID) which uniquely identifies each active segment on a system-wide basis.

The ASID joins the byte number from the PVA to form the SVA which is sent to a cache in local memory.

For further information, refer to Virtual Memory later in this chapter, or to volume 2 of this manual (listed under Related Manuals in About This Manual).

Segment Map Access Validation

The security mechanism in the segment map provides controlled access to all code and data. This protects the operating system from users, users from each other, and users from the operating system.

The basic element of protection is the user's address space, which is the set of addresses the operating system assigns to an executing process. This address space is defined by the set of segment descriptors in the segment descriptor table (SDT) maintained by the operating system. Each segment descriptor defines the security protection features for one segment. The protection features consist of:

- Security ring tests
- Key and lock tests
- Read/write/execute privilege validity tests

For every CM access attempted, all of these tests must be successful. For further information, refer to volume 2 of this manual (listed under Related Manuals in About This Manual).

CM Access Via Segment Map

Segment map contains up to 32 of the most recently used 64-bit segment descriptors from the SDT in CM. The CP tests whether the requested segment descriptor is in segment map on every memory reference.

In this test, the CP uses the lower four bits of the segment number to index 2 of the 32 most recently used segment descriptors. It then compares the requested segment number's upper eight bits to the indexed segments' upper eight bits. If they match, the segment map sends the ASID in this segment descriptor to local memory for the SVA-to-RMA translation. If the segment descriptor is not available in segment map, the CP obtains it from the SDT.

Local Memory

Local memory contains the hardware to translate SVAs to RMAs. To reduce CM access time, the local memory also contains two buffer memories.

- Cache memory
- Page map memory

Cache memory contains 4096 words (32K bytes) of the most recently used entries in the system virtual memory.

Page map contains up to 96 of the most recently used page descriptors from the system page table.

The CP simultaneously tests cache memory and page map to see if the requested SVA is present.

- If a cache memory hit occurs, no further action is required because the CP reads the desired data from cache memory (described in CM Access Via Cache Memory).
- If the desired data is not in cache memory, the page map test is relevant (described in CM Access Via Page Map).
- If a page map hit occurs, the SVA-to-RMA translation completes and the CP reads a four-word block of data from CM (described in Page Map Address Translation).
- If no page map hit occurs, the CP initiates a search of the system page table (SPT).
- If the page is not listed in the SPT, the CP retrieves it from external mass storage.

CM Access Via Cache Memory

Cache memory is a high-speed buffer memory transparent to the user. Since it is a smaller and faster memory than CM, cache memory effectively reduces CM access time by eliminating unnecessary CM references.

On a first reference to a word in CM, the CP rapidly reads a block of four CM words containing the requested word into cache memory. On the subsequent reading of any word in this block, CM need not be accessed because these words are in cache memory. The probability of a cache hit is well over 90 percent for most data processing applications because:

- The same data is often read more than once.
- The CP may repeatedly execute a loop of instruction words.

Cache contains 4096 words (32K bytes) in four 1K word sets.

The CP tests whether the requested entry is in cache on every memory reference comparing the requested entry to the entries in each set. If no cache hit occurs, the CP reads a block of four new words containing the requested entry into the indexed position. The CP uses the entry's lower five address bits to select the requested word, and the byte within that word, from the new block.

On CP writes to CM, the same test is made to determine if data exists in cache. If it does, cache is updated with the new data. If the data is not present in cache, the write operation proceeds with no cache involvement.

Virtual State monitor mode may designate certain virtual memory segments as cache bypass segments. The CP never reads this information into cache memory.

CM Access Via Page Map

If the simultaneous test of cache memory and page map does not produce a cache hit, the page map test is relevant. Page map contains up to 96 of the most recently used page descriptors from the software managed SPT in CM.

The CP tests whether the requested page descriptor is in page map. In this test, the CP uses the lower five bits of the segment/page identifier (SPID) to index the 32 most recently used page descriptors in the SPT.

- If they match (page map hit), page map translates the SVA to an RMA and the CP reads a four-word block of data from CM.
- If no page map hit occurs, the CP initiates a search of the SPT and obtains the page descriptor.

Page Map Address Translation

If no cache or page map hit occurs, page map translates the SVA from segment map to an RMA. Page map performs the translation by hashing (exclusive OR) the ASID and page number to form the SPID. The SPID provides an index into the SPT. From the indexed location, the CP searches the SPT to find the page descriptor with the required SPID.

Along with the SPID, the page descriptor contains a page frame address (PFA), which is the starting address of each page currently in CM. System software uses the PFA to generate the RMA where the requested data resides. For further information, refer to Virtual Memory Programming in volume 2 of this manual (listed under Related Manuals in About This Manual).

Addressing Section

The addressing section has the following functions.

- Forms the byte number portion of the SVA sent to local memory.
- Performs address arithmetic and data manipulation for loading and storing data in CM. The load and store instructions involve transferring a single bit, byte stream, word, or multiple words between register file locations (in the operand issue section) and CM locations.
- Performs the test and set bit instruction, which transfers one bit from a CM location to a specified, constant bit position in an X register.
- Contains address streaming logic for BDP instructions. This includes:
  - Disassembling 64-bit words from local memory into 8-bit bytes for the BDP section
  - Assembling BDP bytes into 64-bit words for local memory

Business Data Processing (BDP) Section

The BDP section executes BDP instructions that operate on CM data fields up to 256 bytes in length. Although the BDP section performs most BDP operations independently, it may require processing assistance from the ALN in the execution section for some operations. BDP operations use any of 12 data types which are organized as follows.

- Packed decimal (4)
- Unpacked decimal (5)
- Binary (2)
- Alphanumeric (1)

In many cases, the data types may be freely mixed as the hardware performs the type translations required for various BDP operations. (Refer to BDP Programming in volume 2 of this manual (listed under Related Manuals in About This Manual) for descriptions of the data types.

BDP instructions reference BDP data via data descriptors, which are in the main instruction stream and which contain information about the location, size, and type of data. The BDP data descriptors also specify two data fields in CM: the source field and the destination field. The source modifies, replaces, or compares to the latter.

Maintenance Access Control (MAC)

MAC performs initialization and maintenance operations in the CP. These operations, controlled by a dedicated PP in the IOU, include the following.

- Initialize registers, controls, and memories
- Read and write CP-resident registers and memories
- Monitor and record CP error/status information
- Verify error detection and correction hardware
- Reconfigure CP
- Clock initialization and tuning

The IOU sends codes to MAC to indicate the operations to be performed and the affected memory device, registers, and addresses. Certain MAC registers contain CP and CM fault isolation information. Other registers control the internal configuration and operation of the CP and verify that errors are properly reported and recorded.

For more detailed information; refer to Maintenance Channel Programming in Virtual State, volume 2, hardware reference manual (listed under Related Manuals in About This Manual).

Dual-CP Operation

In a dual-CP operation, CP-0 and CP-1 operate independently; neither manages the other. The dual-CP configuration has the following characteristics.

- In the CYBER 960 system, CP-1 operates identically to CP-0, executing the entire Virtual State instruction set independently. CP-1 does not support CYBER 170 State operation.
- The CPs share central memory but translate virtual addresses and access CM independently.
- The CPs maintain separate cache, segment map, and page map memories.
- The CPs share Virtual State monitor mode and its interrupt-handling routines.
- The CPs access a common process queue for process dispatching.

The implementation of dual CPs requires some monitor and job mode constraints so that the CPs operate free of conflicts (refer to the following paragraphs).

Monitor Mode Operation

Virtual State monitor mode services requests from both CPs, but monitor mode is unaware of an additional CP in the system. The operating system provides a convention for servicing either CP's monitor mode requests in an orderly, nonconflicting fashion.

When either CP requests monitor mode intervention, the operating system determines whether the request is for interrupt handling or process switching and proceeds accordingly with request processing (refer to the following paragraphs).

Interrupt Handling

Interrupt handling in a dual-CP system is identical to a single-CP system; the CPs exchange and execute independently in job or monitor mode without interference. However, if the CPs issue concurrent monitor mode requests, a software convention determines how these requests are processed (figure 2-6). This convention does the following.

- Assigns a monitor request code (MRC) to each request from either CP
- Establishes groupings of MRCs (request groups) that are associated with specific sets of monitor mode routines (request processors); each request group has its own request processor

Assigning a request processor to a request group allows the monitor mode interrupt handler to simultaneously process unlike requests (as indicated by unlike MRCs).

If the CPs issue concurrent requests which must be handled by the same request processor, monitor mode forces an interlock on one CP until the request processor is available. However, if the CPs issue concurrent requests which can be handled by different request processors, monitor mode can process both requests simultaneously.

For the case of successive requests for the same request processor, monitor mode serializes such requests and executes them when the request processor is available. Some requests never require interlocks; monitor mode processes these as though the process issued a specific request.

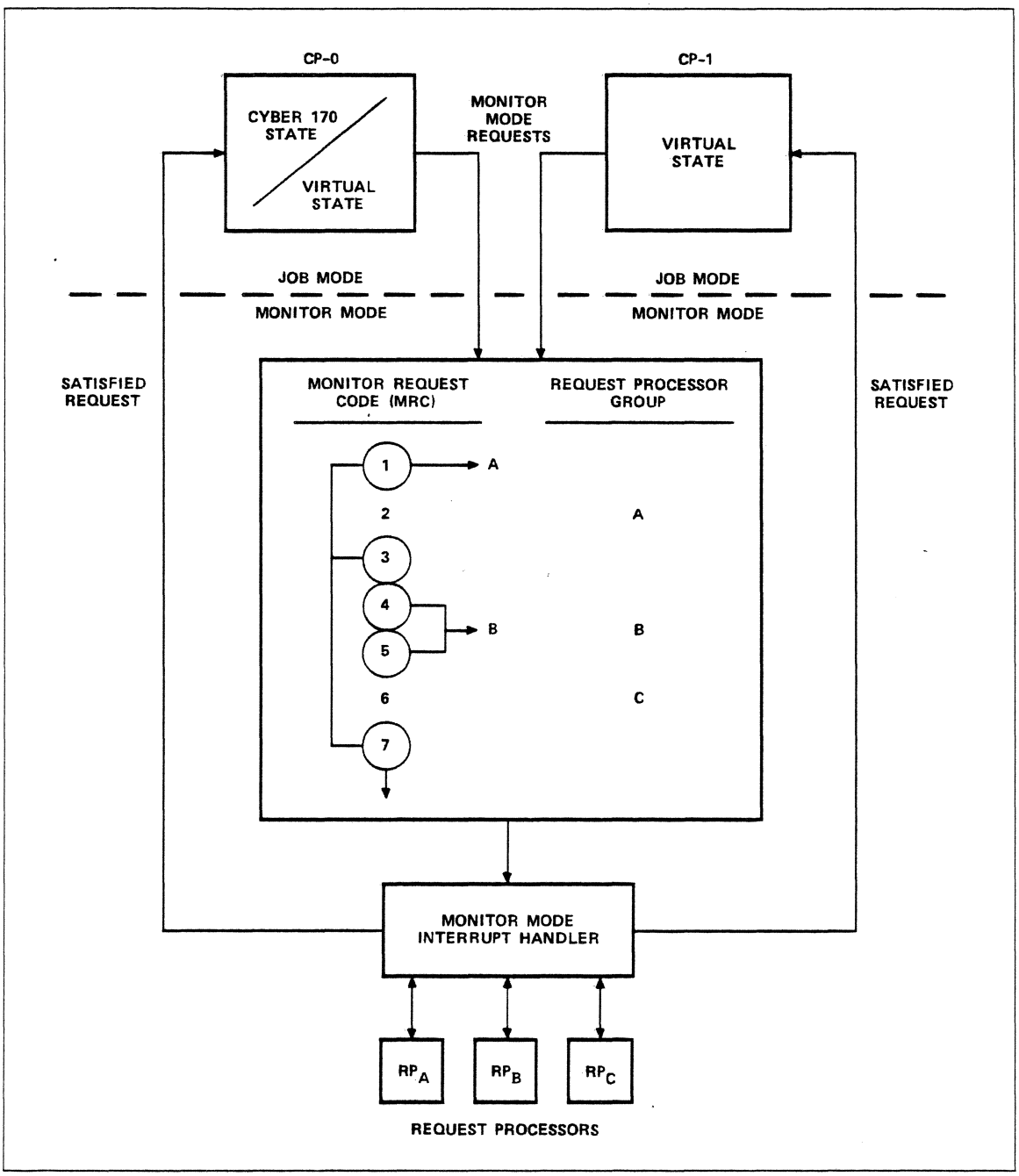


Figure 2-6. Monitor Mode Request Processing in Dual-CP System

Process Switching

Process switching in a dual-CP configuration occurs when:

- One process has executed beyond its execution interval, or
- Process execution has completed.

Monitor mode maintains a collection of task tables describing the state of each process active in the system. A CP request for process switching references the task tables to select a new process from the process queue common to both CPs. The CP then exchanges to job mode to execute it.

Monitor mode process switching routine provides an additional tag to prevent both CPs from simultaneously selecting the same process from the common process queue. The tag, maintained in the task tables, shows which processes are executing, and which are ready to execute.

Job Mode Operation

The dual-CP configuration places few restrictions on job mode operation. These restrictions include the following.

- The operating system ensures that processes do not reference or update exchange packages of other processes.
- Shared data must be located in cache-bypass segments or access to the data must be preceded by a cache-purge operation.
- Because the dual-CP configuration requires fast CP-to-CP communication for page table maintenance, traps in monitor mode must not be disabled frequently or for an extended period of time.

Central Memory (CM)

CM contains the following.

- Eight memory banks that store from 4194K (8388K for CYBER 960) to 32M words with 8-bit SECDED codes
- Multiple ports that make CM accessible to the CP and every PP
- CM bounds register that limits writes to CM from any or all ports
- SECDED generators that generate the SECDED code bits stored with each word and SECDED that checks circuits, corrects single-bit errors, and detects double-bit errors
- Maintenance channel interface that gives a PP in the IOU access to the CM maintenance registers for system initialization, corrective action, error reporting and diagnostics, and for setting the port bounds register

CM Address Format

Figure 2-7 illustrates the address format.

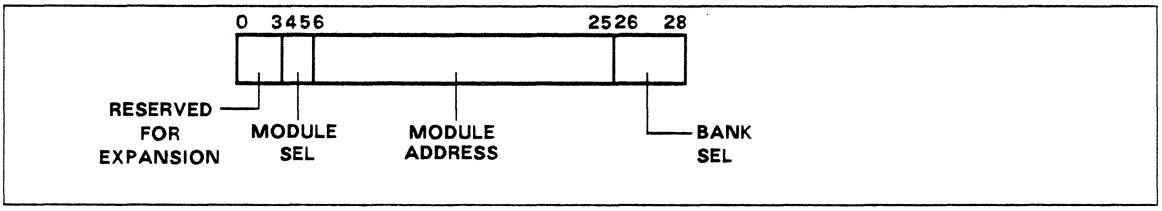


Figure 2-7. Address Format

The following list defines the address fields for figure 2-7.

- Module Select selects one of four sets of memory modules (1 by 1M)
- Module Address internally addresses one location within the memory module
- Bank Select specifies one of eight banks

SECDED

The SECDED logic corrects single-bit errors during a CM read operation, permitting unimpeded computer operation.

The SECDED logic prepares for the error correction by generating error correction code (ECC) bits for each data word and by storing these ECC bits in CM with the data word during the CM write.

Then, during a CM read, CM performs the following SECDED sequence.

1. Reads one CM word and generates new ECC bits for data portion of CM word.
2. Compares new ECC bits with CM word ECC bits.
3. If old and new ECC bits match, no error exists. Sends data to requesting unit.
4. If bits do not match, generates syndrome bits from result of ECC compare.
5. Decodes syndrome bits to determine if single- or multiple-bit failure exists.
6. If single-bit failure exists, corrects by inverting failing bit in data word. Sends corrected word to requesting unit. (Also sets Soft Error Log bit in MCR.)
7. If multiple-bit or other uncorrectable error exists, sends uncorrectable error response code to CP or IOU. (Also sets Detected Uncorrectable Error bit in MCR.) A PP in the IOU may then analyze the syndrome bits using the maintenance channel.

Certain CM registers assist in SECDED analysis.

- The Corrected Error Log (CEL) register displays details of the first corrected error.
- Two Uncorrected Error Log (UEL) registers display details of two different types of uncorrected errors.

For detailed descriptions of these registers, refer to volume 2 of this manual (listed under Related Manuals in About This Manual). The syndrome bits may be analyzed through the maintenance channel.

Table 2-5 lists the hexadecimal codes for all the combinations of syndrome bits with the number of the data bit assigned each code or a note categorizing each code.

CM Bounds Register

The CM bounds register, located in CMC, limits the write access to CM from specified ports. The ports are limited to the area below or above the bounds address as specified in the CM bounds register. Bits in byte 0 specify the port(s) from which the write access is limited, and a bit in the DEC register defines the bounds value as an upper or lower limit. The CM bounds register is set through the maintenance channel. For further information, refer to Maintenance Channel Programming in volume 2 of this manual (listed under Related Manuals in About This Manual).

Table 2-5. SECDED Syndrome Codes/Corrected Bits

Code	Bit	Code	Bit	Code	Bit	Code	Bit
00	1	10	67[2]	20	66[2]	30	2/3[3]
01	71[2]	11	4	21	4	31	6
02	70[2]	12	4	22	4	32	6
03	6/7[3]	13	6	23	6	33	4
04	69[2]	14	4	24	4	34	6
05	4	15	6	25	6	35	4
06	4	16	6	26	6	36	4
07	24[5]	17	3	27	3	37	28[5]
08	68[2]	18	4	28	4	38	6
09	4	19	6	29	6	39	4
0A	4	1A	6	2A	6	3A	4
0B	16[5]	1B	3	2B	3	3B	20[5]
0C	4/5[3]	1C	6	2C	6	3C	4
0D	8[5]	1D	3	2D	3	3D	12[5]
0E	0[5]	1E	3	2E	3	3E	4[5]
0F	4	1F	6	2F	6	3F	4

Notes:

1. No error detected.

2. Check code bit failed (single code bit set).

3. Double error or multiple error or forced double error due to a partial write parity error on one of the two bytes indicated.

4. Double error or multiple error (even number of code bits set).

5. Corrected single-bit error.

6. Multiple error reported as a single error.

(Continued)

Table 2-5. SECDED Syndrome Codes/Corrected Bits *(Continued)*

Code	Bit	Code	Bit	Code	Bit	Code	Bit
40	65[1]	50	2	60	2	70	56[5]
41	2	51	3	61	3	71	4
42	2	52	3	62	3	72	4
43	3	53	2	63	2	73	60[5]
44	2	54	3	64	3	74	4
45	3	55	2	65	2	75	58[5]
46	3	56	2	66	2	76	62[5]
47	4	57	26[5]	67	30[5]	77	4
48	2	58	3	68	3	78	4
49	3	59	2	69	2	79	57[5]
4A	3	5A	2	6A	2	7A	61[5]
4B	4	5B	18[5]	6B	22[5]	7B	4
4C	3	5C	2	6C	2	7C	59[5]
4D	4	5D	10[5]	6D	14[5]	7D	4
4E	4	5E	2[5]	6E	6[5]	7E	4
4F	3	5F	2	6F	2	7F	63[5]

Notes:

1. Check code bit failed (single code bit set).
2. Double error or multiple error (even number of code bits set).
3. Multiple error reported as a single error.
4. Double error or multiple error.
5. Corrected single-bit error.

(Continued)

Table 2-5. SECDED Syndrome Codes/Corrected Bits *(Continued)*

Code	Bit	Code	Bit	Code	Bit	Code	Bit
80	64[1]	90	2	A0	2	B0	48[5]
81	2	91	3	A1	3	B1	4
82	2	92	3	A2	3	B2	4
83	3	93	2	A3	2	B3	52[5]
84	2	94	3	A4	3	B4	4
85	3	95	2	A5	2	B5	50[5]
86	3	96	2	A6	2	B6	54[5]
87	4	97	25[5]	A7	29[5]	B7	4
88	2	98	3	A8	3	B8	49[4]
89	3	99	2	A9	2	B9	49[5]
8A	3	9A	2	AA	2	BA	53[5]
8B	4	9B	17[5]	AB	21[5]	BB	21/53[3]
8C	3	9C	2	AC	2	BC	51[5]
8D	4	9D	9[5]	AD	13[5]	BD	4
8E	4	9E	1[5]	AE	5[5]	BE	4
8F	3	9F	2	AF	2	BF	55[5]

Notes:

1. Check code bit failed (single code bit set).
2. Double error or multiple error (even number of code bits set).
3. Multiple error reported as a single error.
4. Double error or multiple error.
5. Corrected single-bit error.

(Continued)

Table 2-5. SECDED Syndrome Codes/Corrected Bits *(Continued)*

Code	Bit	Code	Bit	Code	Bit	Code	Bit
C0	0/1[1]	D0	40[4]	E0	32[4]	F0	[5]
C1	[2]	D1	40[2]	E1	32[2]	F1	[3]
C2	[2]	D2	44[2]	E2	36[2]	F2	[3]
C3	[3]	D3	44[4]	E3	36[4]	F3	[5]
C4	[2]	D4	42[2]	E4	34[2]	F4	[3]
C5	[3]	D5	42[4]	E5	34[4]	F5	[5]
C6	[3]	D6	46[4]	E6	38[4]	F6	[5]
C7	27[4]	D7	27/46[2]	E7	31/38[2]	F7	[5]
C8	[3]	D8	41[2]	E8	33[2]	F8	[3]
C9	[5]	D9	41[4]	E9	33[4]	F9	[5]
CA	[5]	DA	45[4]	EA	37[4]	FA	[5]
CB	19[4]	DB	19/45[2]	EB	23/37[2]	FB	23[4]
CC	[5]	DC	43[4]	EC	35[4]	FC	[5]
CD	11[4]	DD	11/43[2]	ED	15/35[2]	FD	15[4]
CE	3[4]	DE	3/47[2]	EE	7/39[2]	FE	7[4]
CF	[5]	DF	47[4]	EF	39[4]	FF	[5]

Notes:

1. Double error or multiple error or forced double error due to a partial write parity error on one of the two bytes.

2. Double error or multiple error.

3. Multiple error reported as a single error.

4. Corrected single-bit error.

5. Double error or multiple error (even number of code bits set).

CM Maintenance Registers

The CM contains maintenance registers which hold memory status and error information, and are accessible through the maintenance channel. Table 2-6 lists the CM maintenance registers. Refer to CM Registers in volume 2 of this manual (listed under Related Manuals in About This Manual), for detailed decriptions of these registers.

Table 2-6. CM Maintenance Registers

Register Name	Number of Bits
Bounds Register (BR)	64
Corrected Error Log (CEL)	64
Element Identification (EID)	32
Environment Control (EC)	64
Free-Running Counter (FRC)	48
Options Installed (OI)	32
Status Summary (SS)	6
Uncorrected Error Log 1 (UEL-1)	64
Uncorrected Error Log 2 (UEL-2)	64

Virtual Memory

CM functions as a virtual memory. Virtual memory effectively gives each user a vast, unique address space complete with a copy of the operating system. Actually, most user codes and data reside in external mass storage, and virtual memory code sharing enables the apparent duplication of operating system routines such as FORTRAN compiler, trap handler, and memory manager.

Virtual memory is discussed in the following paragraphs. For information regarding operation of CYBER 170 State (real) memory, refer to the CYBER 170 State Hardware Reference Manual, listed under Related Manuals in About This Manual.

The operating system, with hardware support, manages virtual memory by segmenting virtual-memory code and data, and mapping this information to real-memory pages.

Segments

Segments are units of virtual memory storage (figure 2-8). Each user's executing process operates in a unique virtual address space divided into a number of segments. A maximum of 4096 segments may exist for each process, and over 65 000 segments may exist system-wide for all user processes. Each segment has a capacity of 2000M bytes (262M words); segment size varies according to the amount of information it contains.

In addition to partitioning the virtual-address space, the segment typically provides the natural divisions of code and data in a process. For instance, one segment may hold data files used by the process; another, executable code unique to the process; and another, a duplicate copy of operating system code shared with other users. To optimize the use of real memory, operating system segments which reside in user address space (for example, monitor mode interrupt handler) are shared by several users, and thus conceptually exist as multiple copies in virtual memory.

Segments also play an important role in access protection. Each segment is assigned a set of read, write, and execute attributes which characterize the use of that segment by various users. For further information, refer to Access Protection later in this chapter, or to volume 2 of this manual (listed under Related Manuals in About This Manual).

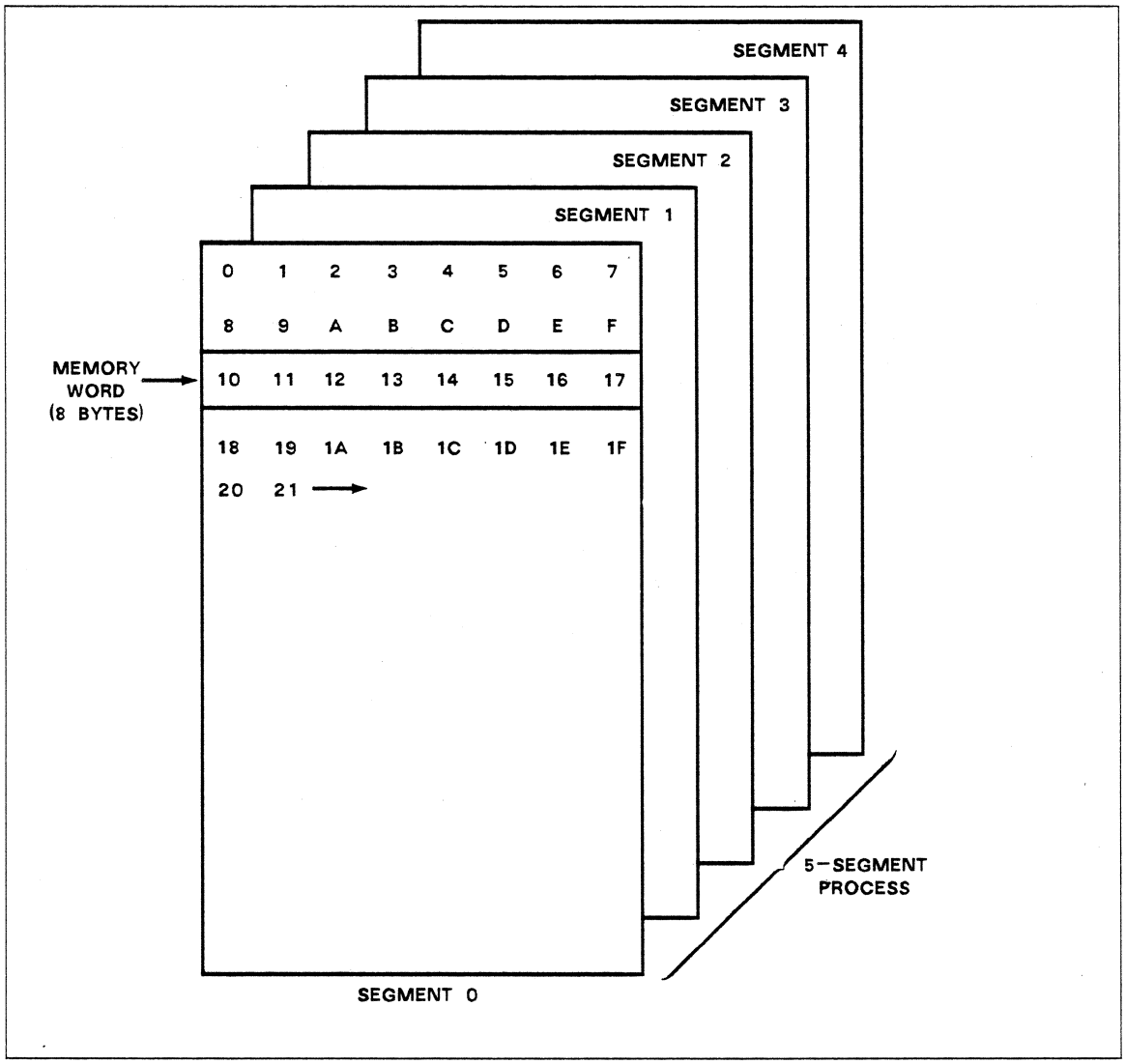

SEGMENT 4
SEGMENT 3
SEGMENT 2
SEGMENT 1
0 1 2 3 4 5 6 7
8 9 A B C D E F
MEMORY WORD (8 BYTES)
10 11 12 13 14 15 16 17
18 19 1A 1B 1C 1D 1E 1F
20 21
5-SEGMENT PROCESS
SEGMENT 0

Figure 2-8. Segments in a Process

Pages

Pages are the units of real memory storage (figure 2-9). Pages also serve as the common storage unit between virtual and real memory. Although pages exist within segments, hardware carries the pages only as bookkeeping in virtual memory. The virtual-to-real page translation facilitates the efficient use of available CM through demand paging and eliminates the need for programmer-created program overlays.

Page size (the number of memory words per page) is of fixed length selected at system initialization and is constant from one deadstart to the next. Pages may be 2K, 4K, 8K, or 16K bytes in length. The number of pages per segment is proportional to page size.

CM comprises physical sections of equal size called page frames. Pages are the same size as page frames; thus, one page of information from external mass storage loads (on demand) into one page frame in CM. A page may or may not reside in CM, depending on its recent use and the competing demand for CM space in retrieving other processes' pages from external mass storage. Many more pages exist in virtual memory than in real memory, and pages are brought from virtual into real memory on a demand basis. Data transfers between CM and external mass storage one page at a time.

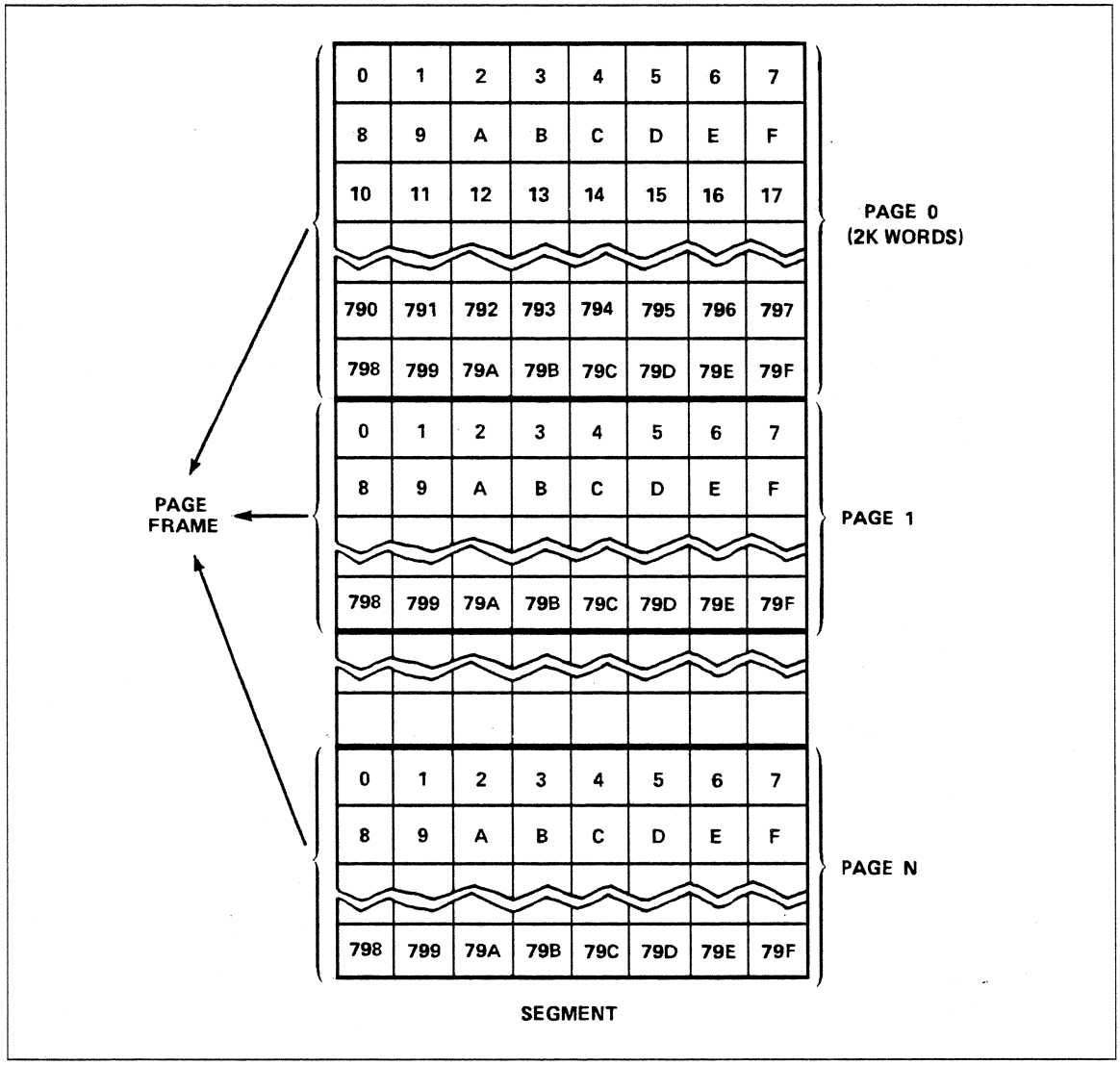


Figure 2-9. Pages in a Segment

Address Translation

CP instructions address memory by way of PVAs. A PVA is the only type of address a user sees. To locate the requested memory word, the CP translates a PVA to a RMA. Hardware performs the translation in two steps by:

1. Converting a PVA to a SVA
2. Converting an SVA to an RMA

The two steps perform distinctly different functions:

- The PVA-to-SVA translation performs a security check which determines whether the process has the necessary privilege to access the requested code/data.
- The SVA-to-RMA translation performs the memory management task of converting the system-wide virtual address to an RMA, which locates the requested code/data in CM or external mass storage. (In the latter, the operating system retrieves the relevant real-memory page from external mass storage into CM.)

The operating system maintains tables in memory which make possible the PVA-to-SVA-to-RMA conversion with access protection (figure 2-10). When translating a PVA to an SVA, the CP uses a software-managed segment descriptor table that describes the unique address space for that segment. When translating an SVA to an RMA, the CP uses the software-managed system page table that contains the page descriptor for each active page in CM.

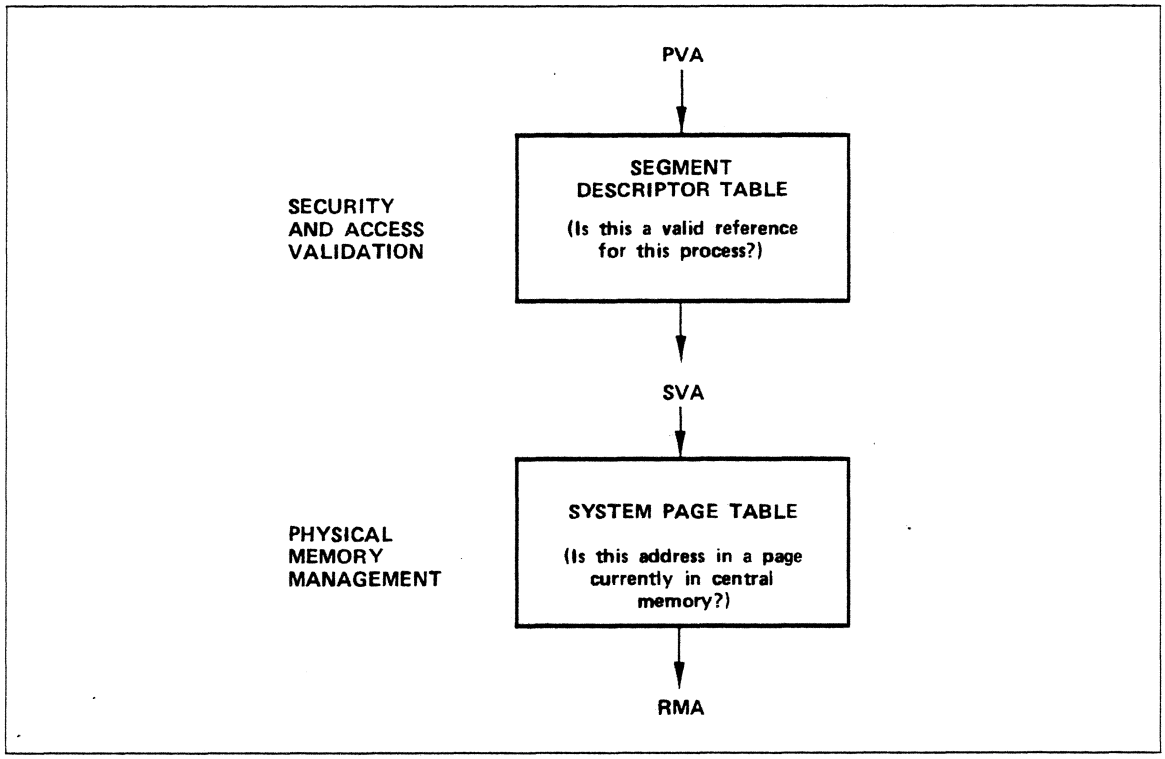


Figure 2-10. Segment/Page Table Role in Address Translation

Access Protection

Access protection consists of constraining each user to an address space and preventing unauthorized reading, writing, or executing of code or data outside this address space. As previously mentioned, the nature of virtual memory allows the operating system to exist in the programmer's address space. Access protection mechanisms are therefore necessary to ensure that protection between system code and user code/data occurs at all times.

The operating system sets access requirements and privileges from information on file or by responding to legitimate requests from the user. The user cannot directly change access requirements or increase access privileges as set by the operating system, because the operating system lists the access requirements of process segments in user-inaccessible areas in CM and places access privilege information with the program counter and address registers.

When the CP presents an address for translation, hardware tests for proper access privilege. Testing of privilege occurs by way of attributes, rings of protection, and keys and locks (described in the following paragraphs). All three tests must be successful, or the CP interrupts the process and performs an exchange to another process. The monitor mode interrupt handler determines appropriate action for the interrupted process.

Attributes

The operating system assigns a set of read/write/execute attributes to each segment; any combination may be assigned. These attributes characterize the use of that segment by various users. The operating system records the attributes in a segment descriptor table for each process and references them at the PVA level of address translation. It is possible for more than one process to share a segment with each process having different access attributes. This forms the basis for code sharing.

When first referencing a PVA, the CP compares the type of reference (read/write/execute) to the attributes of the segment where the PVA resides. To complete the operation, the reference privilege must match a like segment attribute. For instance, reading a particular data segment cannot occur unless the requested segment has a read attribute.

Rings of Protection

The system virtual address space comprises 15 rings of protection. The rings primarily prevent unauthorized access, although rings typically also separate code and data segments. The 15 rings have a hierarchical organization such that the lower the ring number, the higher the privilege. For instance, operating system segments occupy the lowest rings, and the least privileged user segments occupy the highest rings.

Code and data segments for a process may exist in several rings. When this occurs, the segment is said to reside in a ring bracket. There are four ring brackets associated with each segment. These are read, write, execute, and call brackets. The brackets are an extension of the read/write/execute access attributes. On an initial reference to a PVA, the CP compares the ring bracket of the process attempting the read, write, execute, or call to the ring number of the segment where the PVA exists. To complete the access, the referenced segment must reside in an accessible ring bracket.

Keys and Locks

Keys and locks provide a protection mechanism for segments that reside within the same ring of protection. This function includes:

- The protection of local data used by a particular procedure(s)
- The isolation of competing applications residing in the same ring

The CP associates a lock with each segment and, in general, only grants access to one segment from another if the keys exactly match the locks. Thus, this protection mechanism has no hierarchical significance but only depends on whether the keys and locks are the same or different.

Central Memory Control (CMC)

CMC provides a multiple-port interface to CM for the CP and IOU. CMC includes the following.

- Ports and distributor
- SECDED logic which corrects single-bit errors and detects double-bit errors
- Partial-write logic which enables the modifying of an individual byte or bytes within a memory word
- Memory control logic which controls CM reads and writes, and resolves CM bank conflicts and simultaneous CM request conflicts
- Maintenance registers which monitor CM and CMC errors and provides the means for testing and reconfiguring CM for maintenance purposes

Input/Output Unit (IOU)

The IOU performs the functions necessary to locate, select, and initialize the external devices connected to the system and controls the transfer of data between a selected device and CM. The IOU also performs system maintenance functions.

The IOU contains the following functional areas.

- Peripheral processors (PPs)
- I/O channels
- Maintenance channel
- CM access

CYBER 960 IOU and IOU Options

The CYBER 960 IOU consists of the NIO subsystem. The NIO consists of 20 PPs, each having 8K x 16-bit words of memory and a repertoire of 122 instructions. All 20 PPs share access to 24 I/O channels. The PPs are partitioned into four barrels of five PPs.

An optional CIO expansion consists of one or two barrels with five PPs per barrel. Each barrel of the CIO has a group of five DMA I/O channels. With the optional standalone IOU, this can be expanded up to four additional barrels.

CIO PPs have the ability to direct data flow to CM without going through the PP. The data flow is called DMA since it accesses memory directly. DMA allows a higher I/O bandwidth and also allows the PP execution unit to operate independently from the I/O channel during data transfers (concurrently). This concurrency gives the PP more instruction cycle time to process I/O requests from the CP.

CYBER 962 IOU and IOU Options

The CYBER 962 IOU consists of the CIO subsystem containing 10 PPs. Each PP has 8K x 16-bit words of memory and a repertoire of 114 instructions. Each group of five PPs are organized in a time multiplexing barrel and slot system which allows them to share common hardware for arithmetic, logical, and I/O operations without losing speed or independence. With the optional standalone IOU, up to four additional barrels are available.

Each barrel has a set of five dedicated I/O channels. Two of the 10 available channels are dedicated to inter-barrel communication. In addition to the dedicated channels, all PPs have access to special function channels.

The DMA channels can be any combination of ISI, IPI, or CYBER 170 protocols. The ISI adapter transfers data between the ISI channel and CM using standard I/O instructions. The IPI adapter does the same for data transfers between the IPI channel and CM, while the CYBER 170 adapter transfers data between the CYBER 170 channel and CM.

Peripheral Processor (PP)

Each PP can communicate with:

- Other PPs over the I/O channels (subject to restrictions stated previously)
- The CP via CM read and write operations
- The CP (in CYBER 170 State operation) by issuing a CYBER 170 State exchange request to a specific CYBER 170 State exchange package associated with the issuing PP

Each PP can also cause an interrupt condition with the CP operation in either Virtual State or CYBER 170 State.

Each PP executes programs alone or with other PPs to control data transfers between external devices and CM. These programs, called I/O drivers, comprise IOU instructions combined to interact with operating system requests issued through CM.

The I/O drivers translate generalized operating system requests into control functions for accessing the external devices and may also perform device scheduling and optimization.

The NIO I/O drivers use PPM as a buffer for the data transfer between external devices and CM to isolate IOU data transfers from variations in CM transfer rate. The DMA channels can access CM directly and do not require buffer memories.

CYBER 960 PP

The basic CYBER 960 IOU contains 20 NIO PPs and can be expanded to include 5 or 10 CIO PPs. Each PP is a logically independent computer with its own memory (PPM). With the optional standalone expansion, 10, 15, or 20 CIO PPs can be added.

Each five PP group is organized into a mutiplexing system which allows the PPs to share common hardware for arithmetic, logical, and I/O operations without losing independence.

This mutiplexing system comprises five ranks of registers termed a barrel. Each rank contains information related to the instruction being executed by one PP.

Within the NIO subsystem:

- Any PP in a barrel may communicate with any other PP over any of the 23 I/O channels.
- The channels are numbered from 0_8 through 11_8 and 20_8 through 31_8.
- Inter-PP communication is always on a 16-bit boundary.
- The NIO subsystem supports CYBER 170 peripheral equipment (12 bits) using CYBER 170 channel modules.
- Special I/O instructions convert 12-bit channel words to 16-bit PP words, and vice versa.

Within the CIO subsystem:

- PPs within a barrel may communicate with any other PP in the same barrel on any of the five dedicated I/O channels.
- Communication between barrels or with the NIO subsystem must be done by way of special channels.
- Inter-PP communication is always on a 16-bit boundary. The CIO channels are 0_8 through 11_8.

CYBER 962 PP

The basic CYBER 962 IOU contains 10 CIO PPs and can be expanded to contain 15 or 20 CIO PPs. With the standalone expansion, 10, 15, or 20 CIO PPs can be added. Each PP is a logically independent computer with its own memory (PPM).

Within the CIO:

- PPs in different barrels can communicate with each other across the communication channels (0_8, 1_8, 12_8, 13_8).
- PPs in the same barrel can communicate with each other on any of that barrel's dedicated channels or on the common channels (15_8 or 17_8).
- Three different types of DMA-enhanced channels can be installed in any of the available external channel locations. They are the ISI, IPI, and CYBER 170 channels.
- Channels 32_8 and 33_8 are dedicated to SCSI protocol for the DLD.
- The DMA channels are numbered 2_8 through 11_8 and 20_8 through 31_8 and are accessible as follows.
  - Channels 2_8 through 4_8 are accessible by PPs in barrel 0.
  - Channels 5_8 through 11_8 are accessible by PPs in barrel 1.
  - Channels 20_8 through 24_8 are accessible by PPs in barrel 2.
  - Channels 25_8 through 31_8 are accessible by PPs in barrel 3.

Deadstart

There are two methods available for initiating the deadstart sequence. Both methods are accomplished with the system console.

With the first method, selecting System Load Options from the Console Main Menu display initiates the deadstart sequence. With the second method, Maintenance Options is selected from the Console Main Menu display. From Maintenance Options, select System Load With LDS.

The System Load With LDS deadstart sequence is the same as the System Load Options deadstart sequence with the addition of the diagnostic test, LDS. This diagnostic is executed in the IOU and the standalone IOU.

Refer to the 19003 System Console Operations/Maintenance Manual, listed under Related Manuals or the CYBER Initialization Package (CIP) Reference Manual listed under Additional Related Manuals in About This Manual, for more information about the system console and the deadstart sequence.

PP Registers

The PP registers consist of the A, K, P, Q, and R registers. Register descriptions follow.

A Register

The 18-bit A register contains one of two operands for arithmetic and logic operations. The content of A may be:

- Arithmetic operand
- CM address or part of a CM address
- I/O function
- I/O data word
- Word count for a block I/O or CM transfer

Various instructions operate on 6, 12, 16, or 18 bits of the A register. Calculation results are always placed in the A register, although some instructions also write the result into PP memory.

When the A register provides the CM address, parity is generated with the address for transmission to memory control. When the A register provides data or function words for I/O activities, channel parity is always generated on 16 bits of the A register.

At deadstart, the A register is set to 10000_8 for the standard 20 PPs and to 20000_8 for the optional 10 PPs.

K Register

The 7-bit K register is visible to the programmer through the maintenance channel and the IOU deadstart display. This register holds the operation code field of an instruction for display and is used for maintenance purposes. When a PP is halted (idled), this register contains all ones.

P Register

The P register operates in two different modes. In 4K mode, P is a 12-bit register; and in 8K mode, P is a 16-bit register. In 8K mode, the PP memory uses only the least significant 13 bits.

The P register is the PP program address counter. Also, during block I/O and CM transfers, the P register temporarily contains the PP memory address of the data transfer. At deadstart, the P register is set to 7777_8 for the NIO PPs and is set to 1_8 for the CIO PPs.

Q Register

The Q register operates in two different modes. In 4K mode, Q is a 12-bit register; and in 8K mode, Q is a 16-bit register. In 8K mode, the PP memory uses only the least significant 13 bits.

The Q register may hold the following data.

- Operand address for direct and indirect addressing
- Peripheral address of data used during single-word CM read/write instructions
- Shift count
- Word count for CM block transfers
- Upper six bits during constant mode PP instructions
- Target address for relative jump
- Channel number for all I/O and channel instructions

At deadstart, each rank of the Q register is set to a corresponding PP number. Rank 0 is set to PP0, rank 2 is set to PP2, and so on.

R Register

The 22-bit R register, in conjunction with the A register, forms an absolute CM address for CM read/write instruction (refer to Central Memory Access by PPs later in this chapter).

PP Numbering

PPs are numbered in octal as follows. N preceeds NIO PP numbers; C preceeds CIO PP numbers.

Barrel	PPs	Barrel	PPs
CYBER 960		**CYBER 962**	
0	N00 through N04	0	C00 through C04
1	N05 through N11	1	C05 through C11
2	N20 through N24		
3	N25 through N31		
	Optional		*Optional*
0	C00 through C04	2	C20 through C24
1	C05 through C11	3	C25 through C31

The barrels that are located in the standalone IOU and standalone IOU expansion are similar to the CYBER 962 barrels. They are numbered starting at barrel 0 containing PPs C00 through C04 and increment with each additional barrel.

The deadstart sequence decodes a program stored in the IOU microprocessor random-access memory (RAM) to determine PP numbering within a barrel. The sequence:

1. Assigns barrel numbers according to the program.
2. Loads a zero into the Q register in barrel 0 during first minor cycle after deadstart.

This defines all the data in that rank of the barrel as belonging to PP0 and since the Q register is the channel selector, assigns PP0 to channel 0.

During the next minor cycle, the Q register loads with a one. This defines PP1 and assigns it to channel 1.

This process occurs in parallel in all barrels until the IOU assigns each rank of the barrel with a PP number and a channel number. Reassignment can only be done at deadstart. For further information on PP reassignments, refer to the CIP Reference Manual (listed under Additional Related Manuals in About This Manual).

PP Memory

Each NIO PP has an independent 8K word memory degradeable to 4K; each word contains 16 data bits and 6 bits of SECDED code. Each CIO PP has an independent 8K word memory; each word contains 16 data bits and 6 bits of SECDED code.

PP0 reads the deadstart program from the microprocessor RAM during the deadstart operation. Therefore, PP memory 0 must be operational. A PP memory reconfiguration feature allows the user to restore IOU operation if the IOU detects a fault in the PP memory normally assigned to PP0.

To reconfigure, the operator assigns a good PP memory to PP0, and the operating system removes the failing PP memory. Computer operation can continue without the failing PP memory and repairs can be made during scheduled maintenance. The system must be deadstarted to reconfigure PPs.

I/O Channels

The I/O channels comprise an internal interface that allows common hardware and software to control the external devices, and an external interface that allows the IOU to communicate with the external devices using 12/16-bit data channels or an 8-bit maintenance channel.

The internal interface can transfer data between two PPs, or between a PP and an external device at a maximum rate of one word every 250 ns. This rate can be sustained for the maximum practical channel transfer (4096 words). During transfers between PPs, if the PPs are in the slot at the same time, the transfer rate is 500 ns per word.

The external interface contains the interface mechanisms to connect the appropriate channel for an external device. The transfer rate between an I/O device and a PP is a function of the channel type and the maximum data transfer rate of the I/O device.

All PPs communicate with external devices through the independent I/O channels. Each channel may be connected to one or more pieces of external equipment, but only one piece of equipment can use a channel at one time. All channels can be active simultaneously.

Real-Time Clock

The real-time clock is a 12-bit free-running counter, incrementing at a 1-MHz rate. It is permanently attached to channel 14_8. This channel may be read at any time as its active and full flags are always set.

Two-Port Multiplexer

The two-port multiplexer provides a connection between a PP and two RS-232-C communication interfaces. It can simultaneously drive two devices at different baud rates. The two-port multiplexer is permanently attached to channel 15_8.

For a dual-IOU option, both ports of the primary IOU multiplexer are connected to the system console. Only one port of the standalone IOU multiplexer is connected to the same system console, and the other port is not used.

Maintenance Channel

The maintenance channel (MCH) is used for initialization of the CP and CM maintenance registers and monitoring of error status.

The maintenance channel consists of the maintenance channel interface on channel 17_8; a MAC in the CP, CM, and IOU; and a set of interconnecting cables.

Any PP can be programmed to act as the maintenance control unit (MCU). However, hardware dictates PP0 as having special deadstart functions such that PP0 optimally serves as the MCU. In any case, the PP acting as the MCU performs initialization and maintenance functions that include:

- Initializing registers, controls, and memories.
- Monitoring and recording error information.
- Verifying error detection and correction hardware.

The MCU directs these operations by sending function words (instructions) over the maintenance channel to the CP, CM, and IOU. The MCU retains all normal PP capabilities and, except for PP0 deadstart functions, does not gain any special hardware capabilities.

IOU Maintenance Registers

The MAC in the IOU contains several maintenance registers which hold IOU status or error information. Table 2-7 lists the IOU maintenance registers. For detailed descriptions of these registers, refer to IOU Registers in volume 2 of this manual (listed under Related Manuals in About This Manual).

Table 2-7. IOU Maintenance Registers

Register Name	Number of Bits
Element Identification (EID)	32
Environment Control (EC)	32
Fault Status Mask (FSM)	64
Fault Status 1 (FS-1)	64
Fault Status 2 (FS-2)	64
Options Installed (OI)	44
OS Bounds (OSB)	64
Status Register (SR)	32
Status Summary (SS)	6
Test Mode (TM)	16

Central Memory Access by PPs

Any PP can access CM. During a write from the IOU to CM, the IOU assembles four successive 16-bit PP words into one 64-bit CM word (Virtual State), or five successive 12-bit PP words into one 60-bit CM word (CYBER 170 State).

During a CM read, the IOU disassembles a 64-bit CM word into four 16-bit PP words (Virtual State) or a 60-bit CM word into five 12-bit PP words (CYBER 170 State).

To find the CM address, a PP reads the A register. If bit 17 of the A register is clear, the PP uses the contents of the A register for the CM address. If bit 17 of the A register is set, the PP adds the relocation address from the R register to the A register for the CM address.

A maximum of 30 PPs can simultaneously read CM words, and 30 PPs can write CM words.

The OS Bounds register in the IOU is only effective in CYBER 170 State. It contains an enable bit for each PP and an 18-bit bounds address. A set enable bit limits a PP to that area of CM below the bounds address, while a clear bit enables only that area above the bounds address. If the bounds checking is enabled, any write to CM by a PP causes an automatic purge of that address in cache.

Glossary A

Glossary A

A

A Register

Address register.

AC

Address control.

Address

A sequence of bits, a character, or a group of characters that identifies a network station, user, or application.

ADU

Assembly/disassembly unit in the input/output unit.

ALN

Arithmetic/logical network.

Alphabetic character

One of the following letters: A through Z, a through z.

ALU

Arithmetic logic unit.

American Standard Code for Information Interchange (ASCII)

The standard code, using a coded character set consisting of 7-bit coded characters (8-bits including parity check), used for information interchange among data processing systems, data communication systems, and associated equipment. The ASCII set consists of control characters and graphic characters.

AOR

Address out-of-range.

ASCII

See American Standard Code for Information Interchange.

ASID

Active segment identifier.

AUX

Auxiliary.

B

B Register

Index register.

BAS

Barrel and slot in the input/output unit.

BC

Base constant.

BCD

Binary-coded decimal.

BDP

Business data processor.

Binary Synchronous Communications (BISYNC)

A communications term that means running in two directions at alternate times. A bisync line is one that allows a device to both send and receive data.

BISYNC

See Binary Synchronous Communications.

BN

Byte number.

Board

See Logic Module.

BS

Binding section.

BSA

Bit significant address.

BSP

Binding section pointer.

BSR

Bit significant response.

BSS

Bus slave select.

C

Cache

A high-speed memory, duplicating a portion of central memory, used by the central processor to speed memory access.

Carrier

A continuous frequency capable of being modulated or impressed with a signal.

CB

Circuit breaker.

CBP

Code base pointer.

CCEL

Cache corrected error log.

CDC

Control Data Corporation.

CE

Customer engineer.

CEJ

Central exchange jump.

CEL

Corrected error log.

Central Memory (CM)

The main memory of the CYBER 960/962 within the central processing unit cabinet. CM stores between 64 and 256 megabytes of data on 4 to 16 memory modules. CM hardware includes memory modules, a dedicated logic cage, a memory interface module, and voltage regulator modules.

Central Memory Control (CMC)

The logic element in the CPU that controls the movement of data between central memory (CMCA and CMCB) and the central processor. The CMC circuits reside on two logic modules located in the CP-0 logic cage, but accomplish memory control for both CP-0 and CP-1.

Central Processing Unit (CPU)

The main processing cabinet in the CYBER 960 Series mainframe, which includes the central processor (CP-0 and CP-1), central memory control, and central memory. The CPU cabinet has up to two central processors and between 64 and 256 megabytes of resident memory.

Central Processor (CP)

The functional processing logic within the CYBER 960/962 CPU. The first (or standard) central processor is referred to as CP-0. If a second central processor is provided with a system, it is referred to as CP-1. Each central processor resides in a separate logic cage and consists of eleven logic modules.

CF

Critical frame pointer.

CFF

Critical frame flag.

Chan

Channel.

Character

1. Any alphabetic, numeric, or special symbol that can be encoded. This term applies to the graphic characters for a input or output device and to the encoded control characters used by the terminal. Within Control Data hardware, a character is a coded byte of data, such as a 6-bit display code (NOS only) or 7-bit ASCII code. 2. (ISO) A member of a set of elements upon which agreement has been reached, and that is used for the organization, control, or representation of information. Characters may be letters, digits, punctuation marks, or other symbols. A character can be a graphic character or a control character.

CIO

See Concurrent Input/Output.

CIP

CYBER Initialization Package.

CLK

See Clock.

Clock (CLK)

1. (ISO) A device that generates periodic signals used for synchronization. 2. (ISO) Equipment that provides a time base used in a transmission system to control the timing of certain functions such as sampling and the duration of signal elements. See also Real Time.

CM

See Central Memory.

CMC

See Central Memory Control.

CMI

Control memory interface in the input/output unit.

CML

Concurrent maintenance library.

CML/VE

Concurrent maintenance library/virtual environment.

CMM

Central memory multiplexer in the input/output unit.

CMSE

Common maintenance software executive.

Coded Character Set

(ISO) A set of unambiguous rules that establish a character set and the one-to-one relationships between the characters of the set and their coded representation.

Computer room

A room that has a controlled environment that is maintained to meet the requirements of the system equipment.

Concurrent Input/Output (CIO)

An input/output unit architecture that functions with the NOS/VE operating system.

CP

See Central Processor. See also Central Processing Unit.

CP-0

See Central Processor. See also Central Processing Unit.

CP-1

See Central Processor. See also Central Processing Unit.

CPU

See Central Processing Unit.

CRT

Cathode-ray tube.

CSF

Current stack frame.

CSSC

Customer services support center.

CST

Control store.

CST/MAC

Control store/maintenance access control.

CTI

Common test and initialization.

CYBER 960 Series (960/962) Computer Systems

Includes CYBER 960 and CYBER 962 computer systems. The CYBER 960 Series is Control Data's state-of-the-art middle- to high-range system, flanked by the 930 departmental computer on the low end and the 990 computer on the high end of the scalar performance spectrum. A full 960 system includes the mainframe (CPU, IOU, and power unit), MG set, system console, operating software, and a complement of peripherals.

CY170
CYBER 170.

C170
CYBER 170.

D

D/F
Data/function bit.

DC
1. Direct current. 2. Debug code.

DCD
Data carrier detector.

Deadstart
The process of initializing the system by loading the operating system library programs and any of the product set from magnetic tape or disk. Deadstart recovery is reinitialization after system failure.

DEC
Dependent environment control.

Demodulation
The process of retrieving an original data signal from a modulated carrier wave.

Device Interface (DI)
The communcations processor that Control Data offers as its CDCNET hardware product. Also called a CDCNET device interface.

DI
1. Debug index. 2. See Device Interface.

Digit
One of the following characters: 0 1 2 3 4 5 6 7 8 9.

DLD
Dedicated load device.

DLP
Debug list pointer.

DM
Debug mask.

DMA
Direct-memory access.

DMR
Debug mask register.

Down
A status of suspended service.

DRAM
Dynamic random-access memory.

DS
See Deadstart.

DSC
Display station controller.

DSP
Dynamic space pointer.

DSR
Data set ready.

DTR
Data terminal ready.

Dual CP
See Central Processor.

Dual IOU
An IOU installation containing a standard (attached) IOU and a standalone IOU.

Dual State
System capability to run in either/or NOS and NOS/VE.

DUE
Dependent environment control.

DVS
Diagnostic virtual system.

E

EBCDIC
See Expanded Binary Coded Decimal Interchange Code.

EC
Environment control.

ECL
Error correction code. //PUB
Emitter-coupled logic.

ECM
Extended central memory.

ECS

Extended core storage.

EI

Environmental interface.

EIA

Electronics Industries Association.

EID

Element identifier.

EM

Error mode.

EMI

Electromagnetic interference. Synonomous with Radio Frequency Interference.

EPF

External procedure flag.

EQ

Equal.

ES

End suppression toggle (BDP edit instruction).

ESD

Electrostatic discharge.

ESM

Extended semiconductor memory.

ESM-II

Extended semiconductor memory II.

Expanded Binary Coded Decimal Interchange Code (EBCDIC)

The set of 256 characters, each presented by eight bits, that is used with the 3270 Binary Synchronous Communications protocol.

EXT

External.

F

FCC

Federal Communication Compliance.

FCO

Field change order.

FCTN

Function.

Federal Communication Compliance (FCC)

This equipment generates, uses and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device (insert peripheral computing device if appropriate) pursuant to Subpart J of Part 15 of the FCC Rules which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

FF

See Flip-Flop.

Field-Replaceable Unit (FRU)

Equipment parts that are replaceable at the customer site are referred to as FRUs. Equipment manuals generally recommend a list of FRUs that should be stocked on site for that equipment. FRUs are identified with 8-digit part numbers that can be ordered from Control Data's World Distribution Center (WDC). See also World Distribution Center.

FIFO

See First-In/First-Out.

First-In/First-Out (FIFO).

1. This term applies to data processing services in which requests are serviced in the same order they are received. 2.(ANDIPS) A queuing technique in which the item that has been in the queue for the longest time is the next to be processed.

FL

Field length.

FLC

Central memory field length register.

FLE

Extended core storage field length register.

Flip-Flop

(ANDIPS) A circuit or device containing active elements, capable of assuming either one of two stable states at a given time. Synonymous with bistable circuit, toggle (1).

Floating-Point Base

(ISO) In a floating-point representation system, the implicit fixed positive integer base, greater than unity, that is raised to the power explicitly denoted by the exponent in the floating-point representation or represented by the characteristic in the floating-point representation and then multiplied by the fixed-point part to determine the real number represented, e.g., in the floating-point representation of the number 0.0001234, namely 0.1234-3, the implicit floating-point base is 10. Synonymous with floating-point radix.

FP

Floating-point. See Floating-Point Base.

FRC

Free-running counter.

Frequency converter

A motor generator mounted within its control cabinet.

FRU

See Field-Replaceable Unit.

FS

Fault status.

FU

Functional unit.

G

G/L

Global/local.

Graphic Character

(ISO) A character other than a control character, that is normally represented by a graphic.

H

Hardware

1.(ISO) Physical equipment as opposed to programs, procedures, rules, and associated documentation. 2. Electronic circuits and its housing, including cabinet, power hook-up, and cooling system.

Hdr

Header.

Hertz (Hz)

A measure of frequency or band width the same as cycles per second.

HEX

See Hexadecimal.

Hexadecimal

(ISO) Synonym for sexadecimal. See also Sexadecimal.

HPA/VE

Hardware performance analyzer/virtual environment.

Hz

See Hertz.

I

I/F

See Interface.

I/O

Input/output.

IC

Integrated circuit.

ICC

Instruction completion control.

ICP

Instruction control pipe.

ID

1. Identification. 2. Identifier.

IDX

Index.

IF

Instruction fetch.

ILH

Instruction look-ahead.

Input/Output Unit (IOU)

IOU contains the peripheral processors and channels that enable operator interaction with, and peripherals access to, the central processing unit. The IOU has either NOS and NOS/VE capability (CYBER 960) or is NOS/VE only (CYBER 962). The IOU has the interface port for the system console.

INSTR

Instruction.

Interface

1. A shared boundary. An interface might be a hardware component to link two devices or it might be a portion of storage or registers accessed by two or more computer programs. 2. See data transmission interface.

International Standards Organization (ISO)

A worldwide standards group similar in function to the American National Standards Institute (ANSI). ANSI is a member of the International Standards Organization.

IOU

See Input/Output Unit.

IOU Expansion

An add-on IOU product that physically attaches to the CYBER 960 IOU. The IOU expansion is a concurrent input/output (CIO) architecture and allows for addition of up to ten peripheral processors and ten channels. The IOU expansion is the first IOU option to be added to a CYBER 960 mainframe, increasing the number of IOU cabinets to two.

IPI

Intelligent peripheral interface channel architecture in the IOU.

ISI

Intelligent standard interface channel architecture in the IOU.

ISO

See International Standards Organization.

J

JPS

Job process state.

K

K Register

Operation code register.

KEY

Key.

L

Large-Scale Integrated Circuit

A chip that contains around 100 to 1000 logical gates.

LDS

Literature Distribution Services.

LED

Light-emitting diode.

LM

See Local Memory.

LMA

See Local Memory.

LMB

See Local Memory.

LOC

Local.

Local Memory (LM)

The storage area with accompanying control that provides a high-speed interface between the central processor and central memory. LM is contained by two logic modules, LMA and LMB. See also Cache.

LOCK

Lock.

Logic Module

A printed-circuit board with microcircuit chips.

Long Warning (LW)

The power unit generates an LW when an emergency power shutdown is to occur in approximately 1 minute if the fault is in an IOU or in approximately 2 minutes if the fault is in the power unit, CPU cabinet, or with ambient room temperature (assuming the detected fault continues).

LPID

Last processor identification.

LRN

Largest ring number.

LSB

Least significant bit.

LSI

See Large-Scale Integrated Circuit.

LW

See Long Warning.

M

MA

Monitor address.

MAC

Maintenance access control.

MAF

Maintenance action form.

Mainframe

Includes the central processing unit, input/output unit, and power unit portions of the mainframe complex. The mainframe does not include the motor-generator set or the system console.

Mainframe Complex

The hardware products that make up a central processing computer system are referred to collectively as the mainframe complex. Includes the central processing unit, input/output unit, power unit, system console, and the motor-generator set. Peripherals are not included in the mainframe complex.

MAINT

Maintenance.

MALET

Maintenance application language for equipment testing.

MCEL

Map corrected error log.

MCH

Maintenance channel.

MCR

Monitor condition register.

MCU

Maintenance control unit.

MD

Multiply/divide.

MDD

Monitor display driver.

MDF

Model-dependent flags.

MDW

Model-dependent word.

MEJ

Monitor exchange jump.

Memory Interface Module

The logical assembly interfacing central memory and central memory control. The memory interface module is physically attached to the rear of the central memory logic cage and includes circuits for data, addressing, and control.

Memory Module

The logical assembly upon which data is stored in central memory. Four memory modules constitute one memory increment or 64 megabytes of data storage. The central processing unit's central memory contains a minimum of four memory modules and a maximum of 16.

Meter

A unit of measure in the metric system that is equal to 39.3 inches.

MF

Monitor flag.

MG

See Motor-Generator Set.

Micrand

Control store word.

MMR

Monitor mask register.

Modem

(ISO) A functional unit that modulates and demodulates signals. One of the functions of a modem is to enable digital data to be transmitted over analog transmission facilities. Modem is a contraction of modulator-demodulator.

Modulation

A message signal that is impressed on a carrier signal and transmitted at another signal frequency.

Module Assembly

The circuit boards in the CP. There are 13 different modules in the CP.

Mon Cond

Monitor condition.

MOP

Micro-operator (BDP edit instruction).

MOS

Metal-oxide-semiconductor.

Motor-Generator (MG) Interface Unit

The electrical box that interfaces with the motor-generator set. Also see Motor-Generator (MG) Set.

Motor-Generator (MG) Set

A motor generator and a separate motor-generator control cabinet that converts 3-phase site utility power to 3-phase, 400-Hz power suitable for the mainframe electrical requirements. Smaller MG sets may include the MG and its MG control functions within one cabinet and be referred to as a frequency converter.

MPS

Monitor process state pointer.

MR

Maintenance register.

MSB

Most significant bit.

MSG

Message.

MSL

Maintenance software library.

Multiplexer (MUX)

Equipment that enables a site to concentrate data transmission between multiple slower-speed devices (such as, terminals and workstations) and a higher-speed channel. For example a multiplexer can concentrate data being transmitted between multiple terminals and an host computer by using a local area network.

Must

A mandatory requirement.

MUX

See Multiplexer.

N

Network Operating System (NOS)

An operating system for the host computer. It has network capabilities for time-sharing and transmission processing in addition to local and remote batch processing. NOS controls the computation of programs submitted through remote terminals and maintains normal batch processing operations for jobs submitted locally.

Network Operating System/Virtual Environment (NOS/VE)

An operating system for the host computer. It has network capabilities for time-sharing and transmission processing in addition to local and remote batch processing. NOS/VE operates in Virtual State and controls the computation of programs submitted through remote terminals and maintains normal batch processing operations for jobs submitted locally.

NIO

See Nonconcurrent Input/Output.

NOS

See Network Operating System.

NOS/VE

See Network Operating System/Virtual Environment.

NPA

Network performance analyzer.

NS

Negative sign toggle.

O

OCF

On-condition flag.

OI

Options installed.

ON

Occurrence number.

Opcode

Operation code.

Operand Issue (OPI)

That portion of the central processor responsible for storage and distribution of the process state register values while a process is executing. OPI is contained by logic modules OPIA, OPIB, and OP/SM.

OPI

See Operand Issue.

OPI/SM

Operand issue/segment map.

Optl

Optional.

OS

Operating system.

P

P/N

Part number.

P Register

Program address register.

PAR

Parity.

PCB

Printed-circuit board. See Logic Module.

PE

Parity error.

PFA

Page frame address.

PFS

Processor fault status.

PID

Processor identifier.

PIT

Process interval timer.

PM

See Preventive Maintenance.

PMF

Performance monitoring flag.

PN

Page number.

PND

Process-not-damaged flag.

PO

Page offset.

PONR

Point of no return.

Port

The physical connection on the device interface through which data is transferred to/from the device interface. Each port is numbered (labeled) and supports a single communication line.

Power unit

Provides power to support the electrical systems (logic, environmental, and so on) of the CPU. (The IOU has its own power supply.) The power unit occupies a cabinet that attaches to the CPU.

PP

Peripheral processor.

PPM

Peripheral processor memory.

Preventive maintenance

1. (ISO) Maintenance performed specifically to prevent faults from occurring. 2. Contrast with corrective maintenance.

Primary IOU

The IOU cabinet(s) bolted to the CPU; the IOU and, if present, the IOU non-standalone expansion.

PROM

Programmable read-only memory.

PSA
Previous save area pointer.

PSF
Previous stack frame.

PSM
Page size mask.

PSWF
Page search without find.

PTA
Page table address.

PTE
Page table entry.

PTL
Page table length.

PTM
Processor test mode.

PVA
Process virtual address.

PWR
Power.

Q

Q Register
Operand address register.

R

RAC
Central memory reference address register.

RAE
Extended core storage reference address register.

RAM
Random-access memory.

RDS
Register/data select.

Real Time

Pertaining to the processing of data by a computer in connection with another process outside the computer according to time requirements imposed by the outside process. This term is also used to describe systems operating in conversational mode and processes that can be influenced by human intervention while they are in progress.

Real-time clock

See Real Time and Clock.

REM

Remote.

RESP

Response.

Resync

Resynchronize.

RGTR

Register.

RI

Radial interface.

RMA

Real-memory address.

RN

Ring number.

RP

Ring number indictor. //PUB

Read permission.

ROM

Read-only memory.

RS-232-C

An Electrical and Electronic Industries Association (EIA) standard that describes the interface between terminals or other data terminal equipment and modems or other data communications equipment employing a serial binary interchange.

RTA

Remote technical assistance.

RTC

See Real-Time and Clock.

RTS

Request to send.

S

SCD

System console driver.

SCSI

Small computer standard interface in IOU. The system console interfaces with the IOU through SCSI.

SCT

Special characters table.

SDE

Segment descriptor table entries.

SDT

Segment descriptor table.

SECDED

Single error correction/double error detection.

Secondary IOU

The IOU cabinet(s) not bolted to the CPU; the standalone IOU and, if present, the standalone IOU expansion.

SEG

Segment.

Sexadecimal

1. (ISO) Characterized by a selection, choice or condition that has sixteen possible different values or states. 2. (ISO) Of a fixed-radix numeration system, having a radix of sixteen. 3. Synonymous with hexadecimal.

SFSA

Stack frame save area.

Short Warning (SW)

The power unit generates on SW when an emergency power shutdown is to occur in 2.5 seconds. Also see Emergency Power Shutdown.

Should

A recommendation that is advised but not required.

SIB

See Side Interconnect Board.

Side Interconnect Board (SIB)

SIBs are the printed-circuit boards that interconnect the central processor logic modules. The multilayered SIBs actually constitute the sides of the CP logic cages. CP-0 logic modules are interconnected with SIB A and SIB B, while CP-1 logic modules are interconnected with SIB C and SIB D.

Single processor

See Central Processor.

SIT

System interval timer.

Site

The computer room and other building locations that may include one or more motor-generator sets and data media storage.

SLAVACK

Slave acknowledge.

SM

1. Segment map. 2. Symbol.

SMA

Standardized maintenance approach quick reference.

SN

Negative sign.

SPID

Segment page identifier.

SPM

System power monitor.

SPT

System page table.

SR

Select reset.

SRT

Subscript range table.

SS

Status summary.

STA

Segment table address.

Stack

An area in memory used as temporary storage for chaining calls during task or interrupt service routine execution. Task calls are chained on a user stack. Interrupt service routine calls are chained on a supervisor stack.

Stack Frame

The area within a stack that accommodates a single call.

Standalone IOU

The standalone IOU is an option that provides the CYBER 960/962 mainframe with a dual IOU configuration. The standalone IOU is installed on an island separate from the mainframe, but is linked to the CYBER 960/962 CPU with 50-ft cables. Up to ten peripheral processors (PPs) and ten channels reside in the standalone IOU cabinet.

Standalone IOU Expansion

A standalone IOU expansion product can be added to the standalone IOU, doubling the PP and channel capability of the standalone IOU configuration. The standalone IOU expansion and the IOU expansion differ only in their physical location relative to the mainframe.

STL

Segment table length.

SV

Specification value.

SVA

System virtual address.

SW

See Short Warning.

System Console

The keyboard and display screen used to monitor and control the operating system.

T

T'

T-prime register.

TE

Trap enable.

TED

Trap-enable delay.

TEF

Trap-enable flip-flop.

TER

Terminate.

TM

Test mode.

TOS

Top of stack.

TP

Trap pointer or test point.

TPM
Two-port multiplexer.

U

UART
See Universal Asynchronous Receiver/Transmitter.

UCR
User condition register.

UEL
Uncorrected error log.

UEM
Unified extended memory.

UMID
Untranslatable virtual machine identifier.

UMR
User mask register.

Universal Asynchronous Receiver/Transmitter (UART)
An LSI circuit for start/stop serial data transfer.

User Cond
User condition.

UTC
Utility channels.

UTP
Untranslatable pointer.

UVMID
Untranslatable virtual machine identifier.

V

V
1. Valid bit. 2. Also see Volt.

VC
Search control code.

VL
Segment validation.

VMCL
Virtual machine capability list.

VMID
Virtual machine identifier.

Volt (V)
A measure of the work needed to move an electric charge.

W

WDC
See World Distribution Center.

World Distribution Center (WDC)
Control Data's ordering and distribution center for spare hardware parts, software revision packages, and the documentation produced to support its product lines.

WP
Write access control (segment descriptor field).

WR
Write/read.

X

X Register
Operand register.

XP
Execute access control.

Z

ZF
Zero field toggle.

ZFI
Zero-fill inhibit.

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